

What's a Computer?

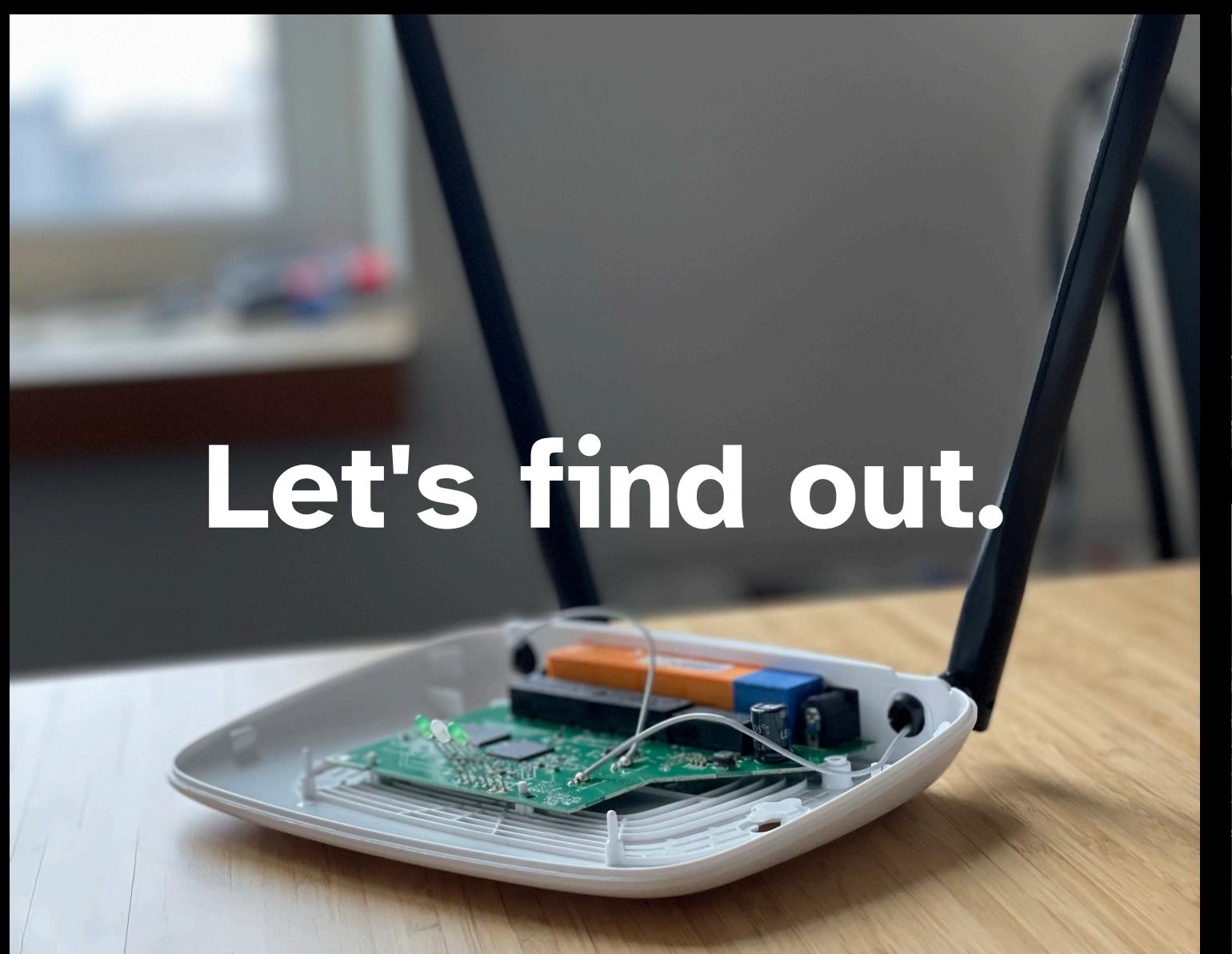
Processor

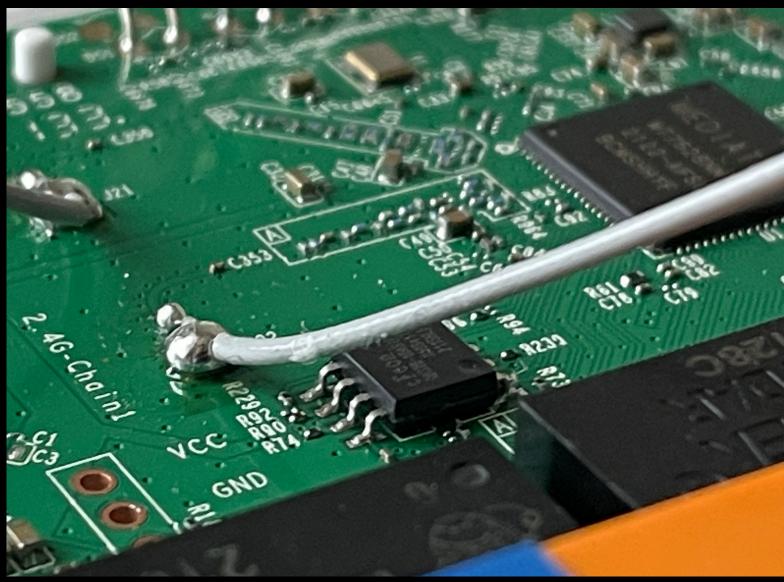
What's a Computer?

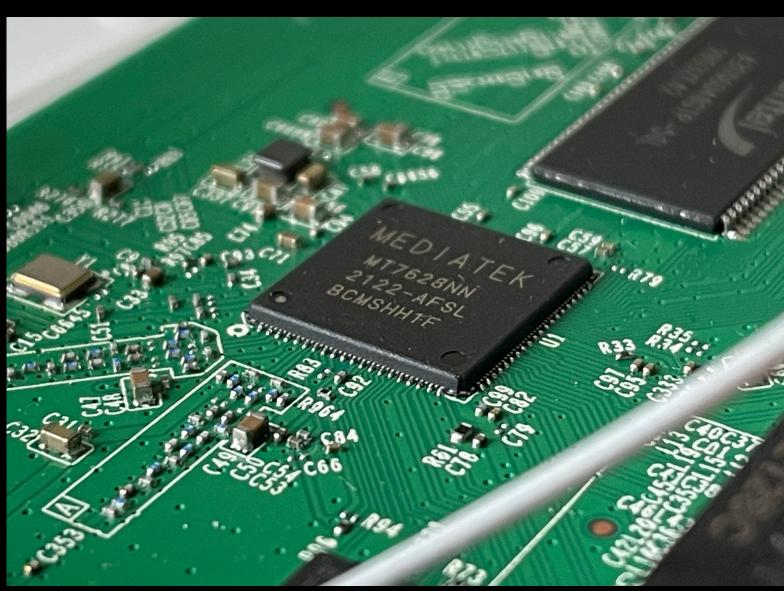
Memory

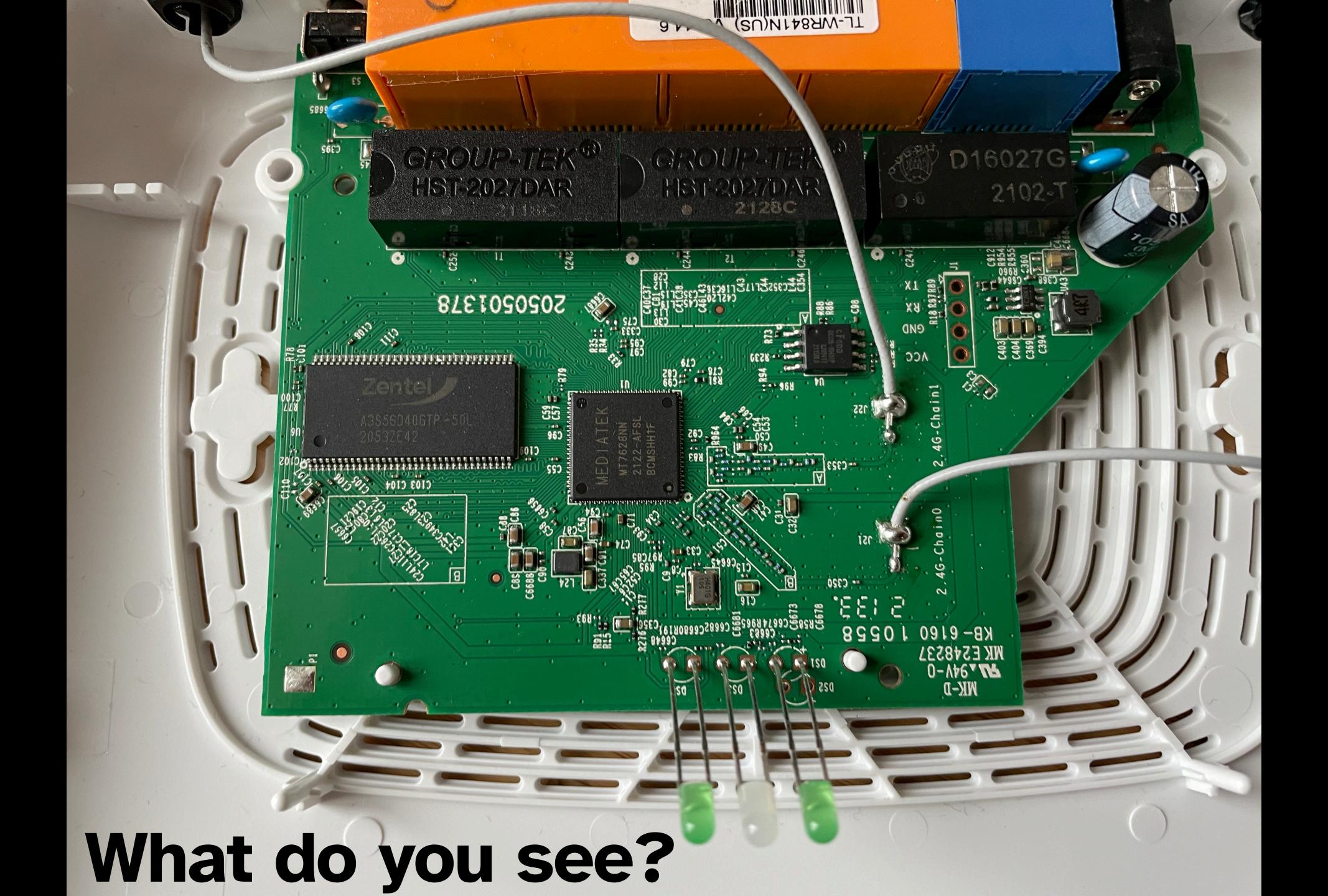
Storage

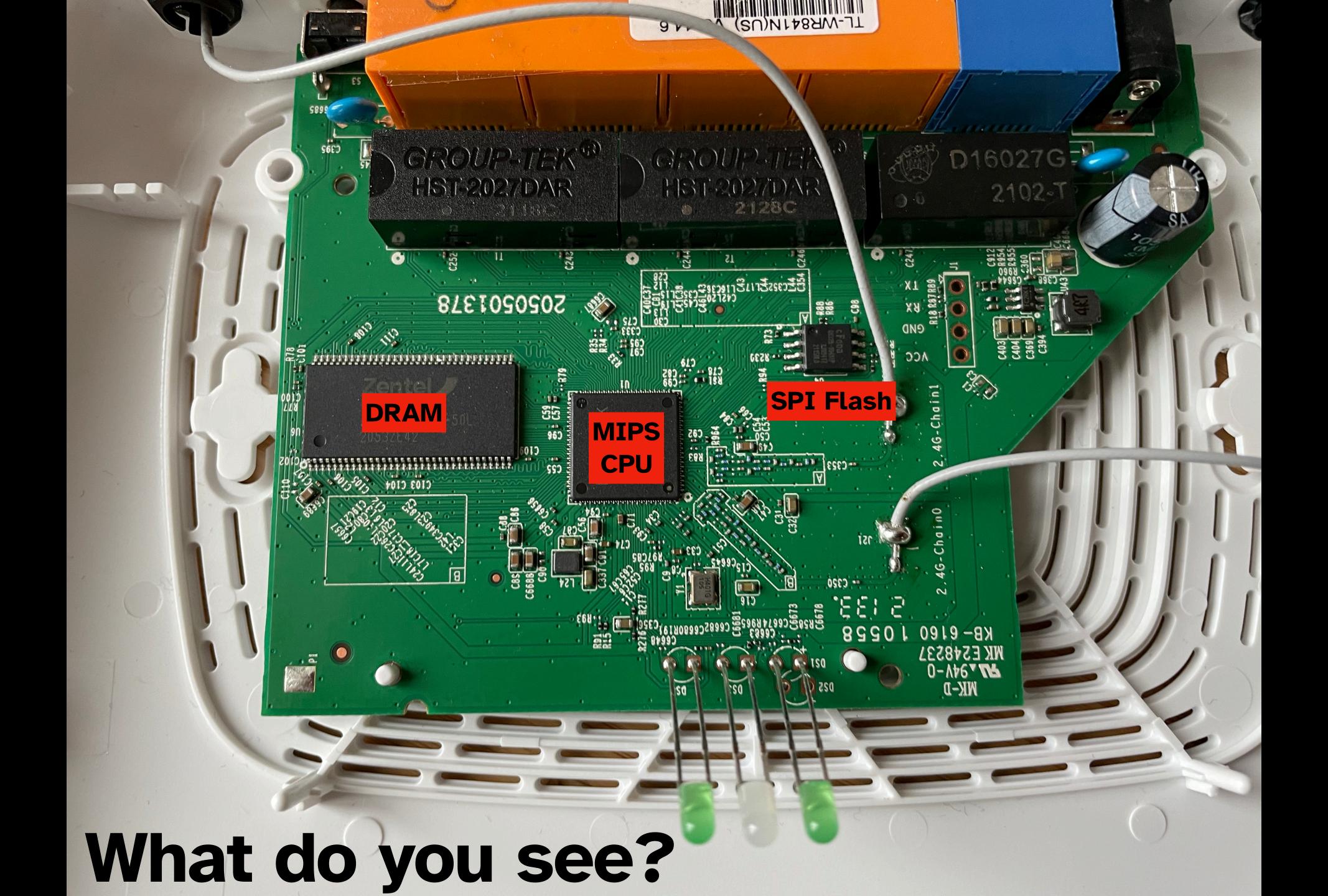


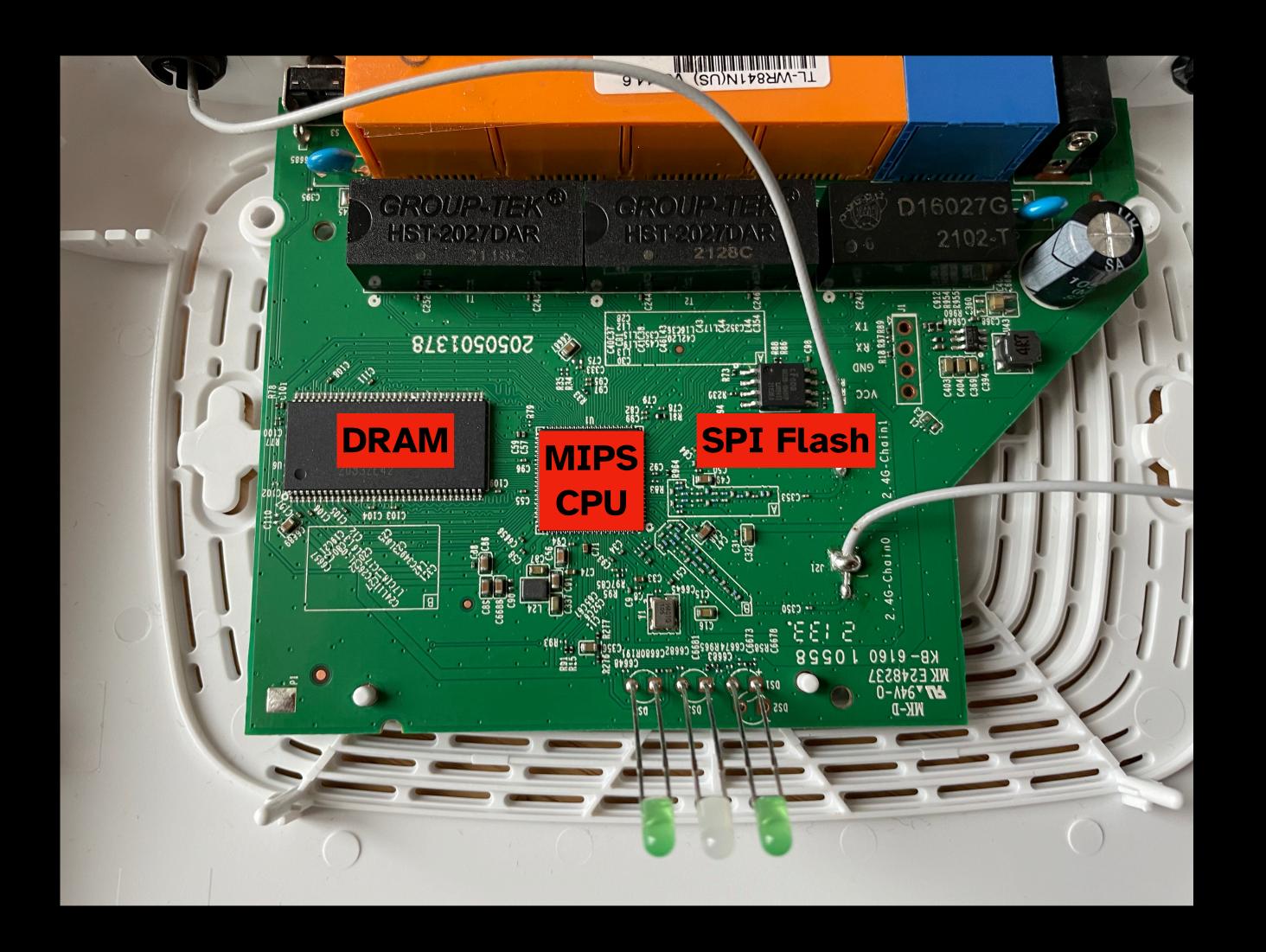








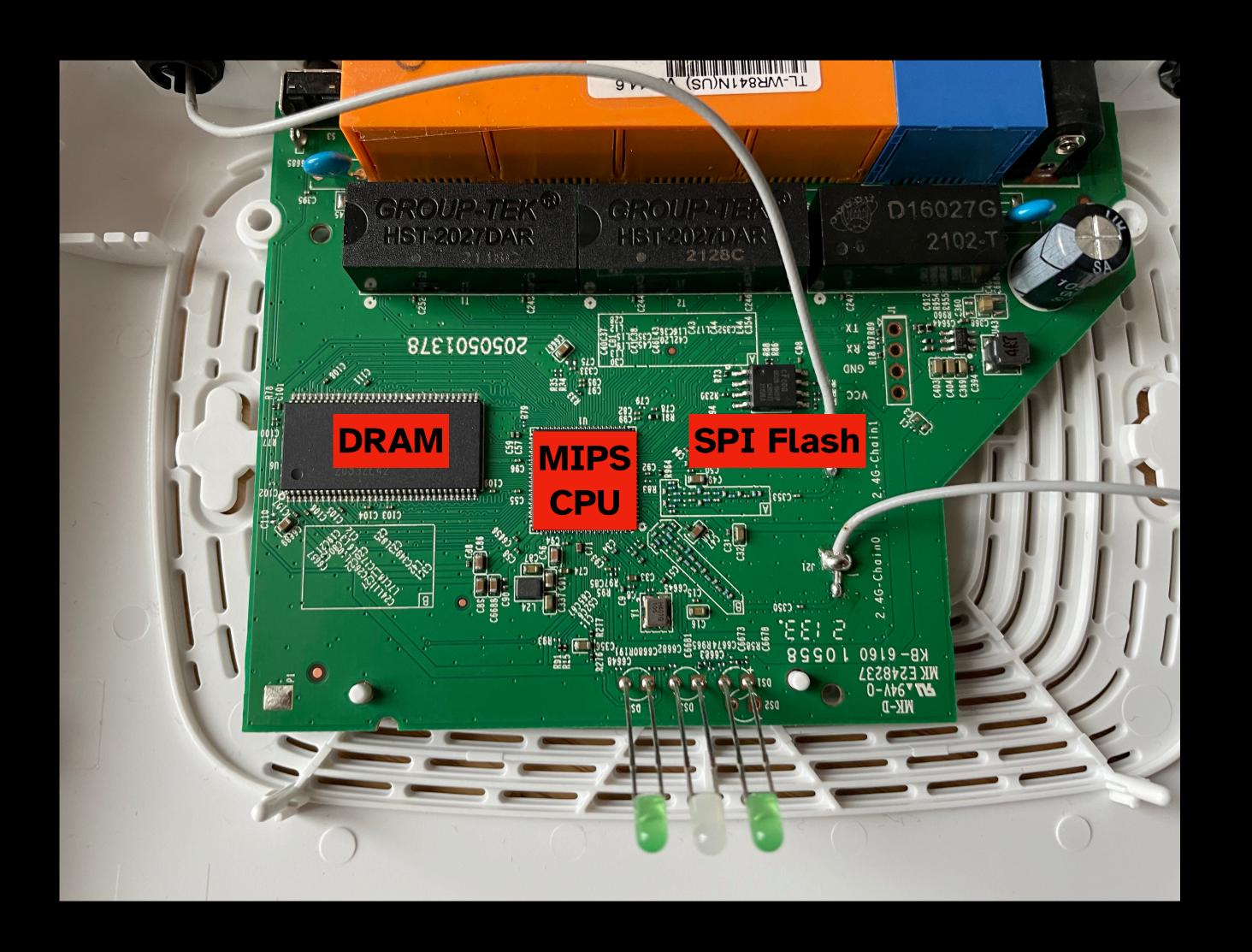




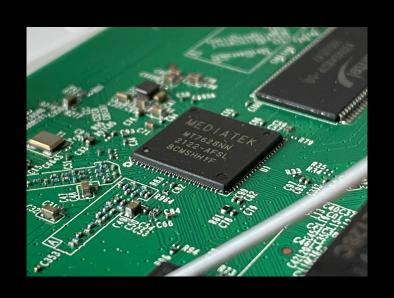
Processor

Memory

Storage



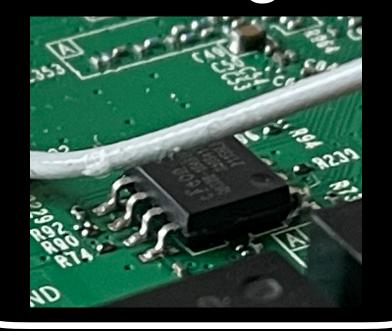
Processor

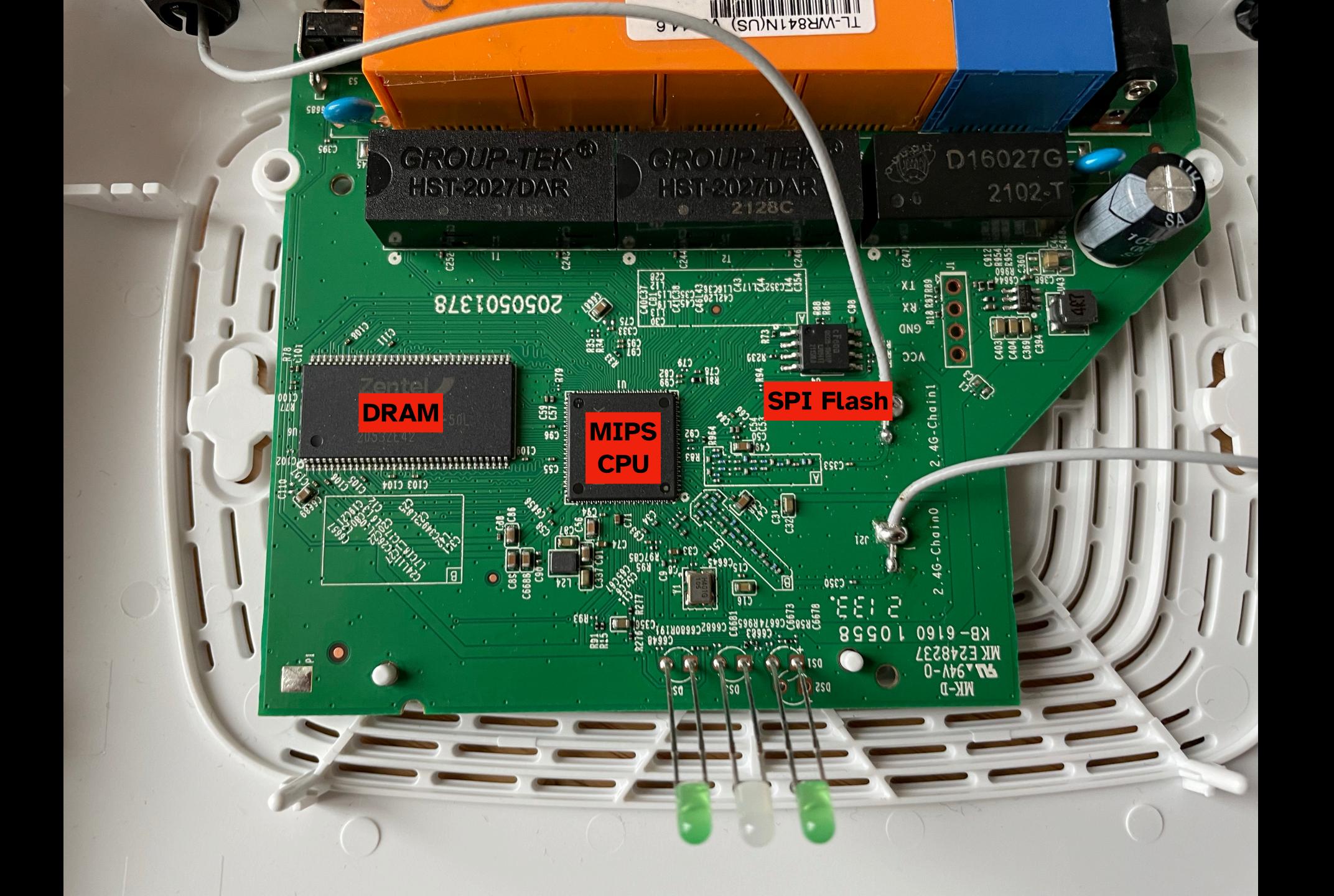


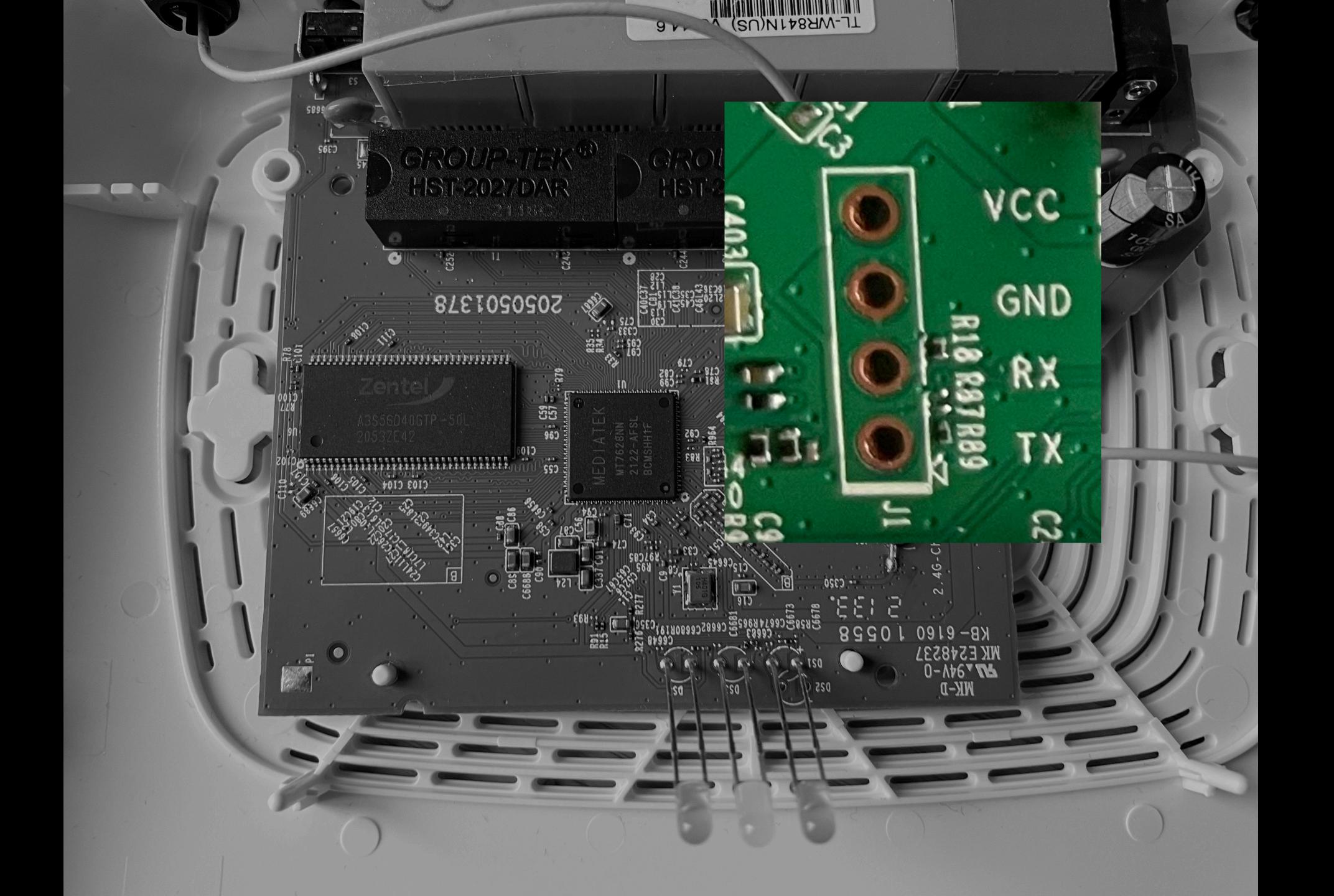
Memory

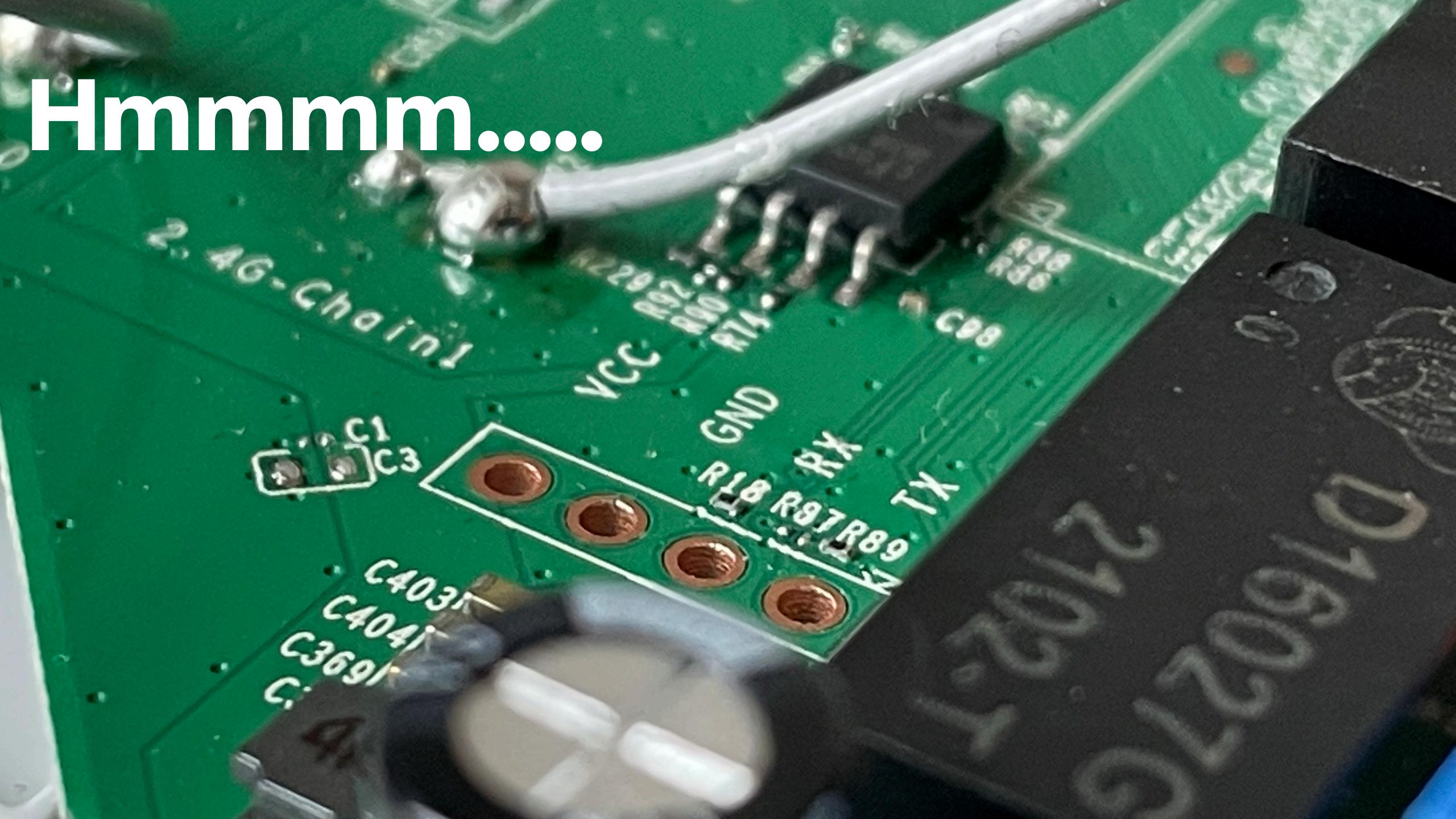


Storage







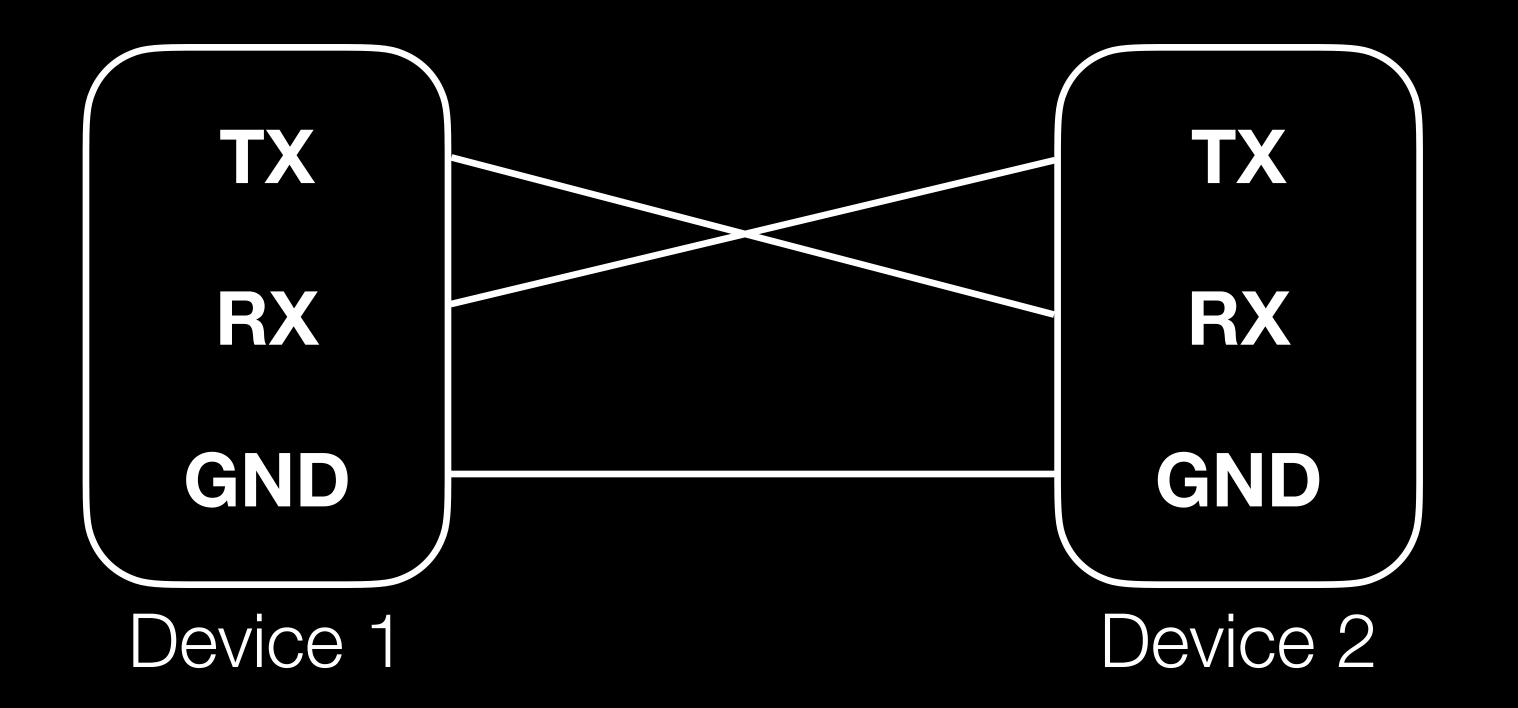


Demo 1

"What if the vendor just leaves the backdoor open?"

UART

Universal Asynchronous Receiver/ Transmitter





What other interfaces are out there?

UART/USART

Serial Protocol, a lot of the times just gives a root shell for free

JTAG/ SWD

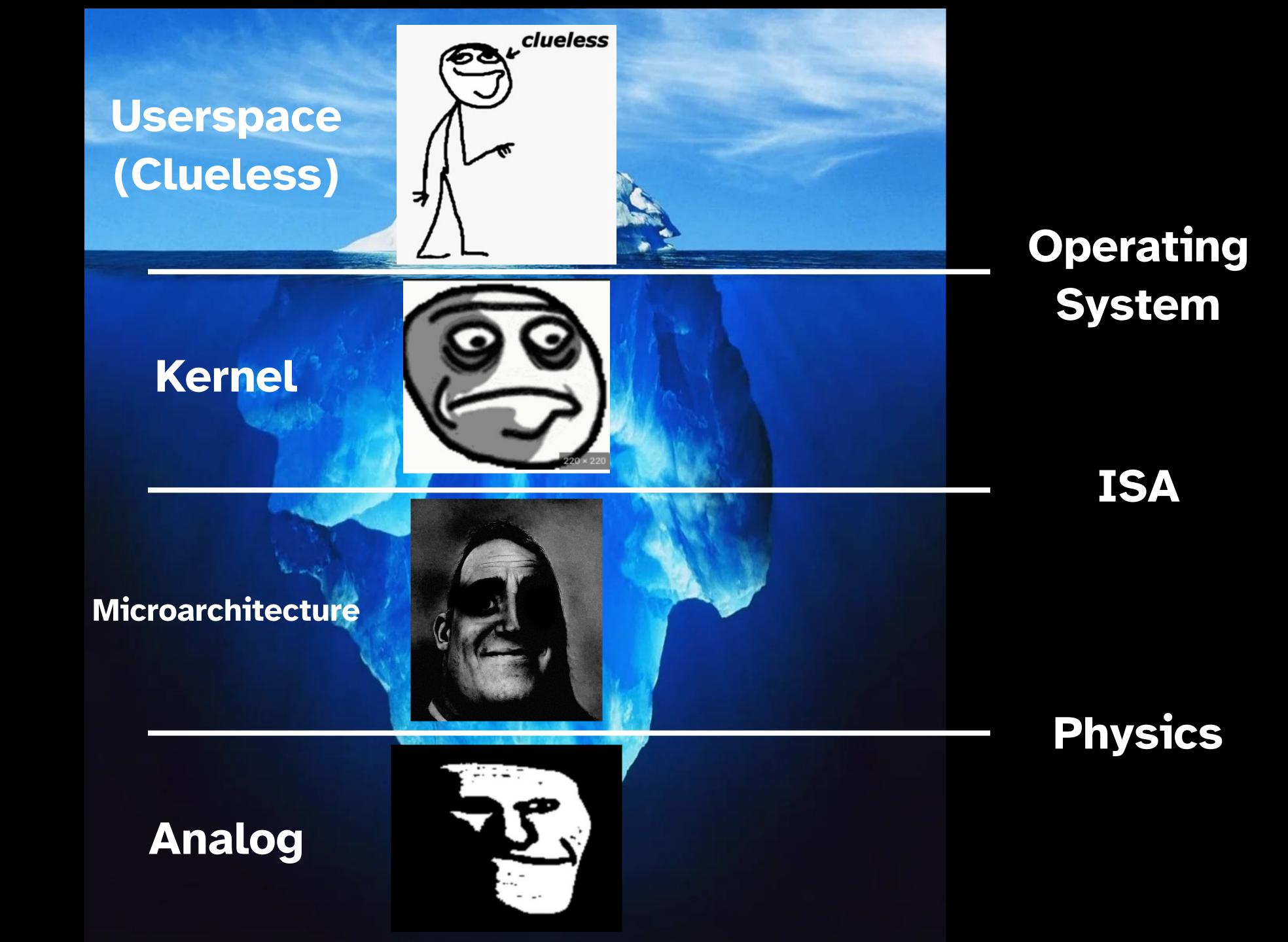
Dump firmware, debug CPU, upload your own firmware

I2C/ SPI

Protocol used to let chips talk to each other. PC BIOS uses SPI.



The HW Security Iceberg



Active

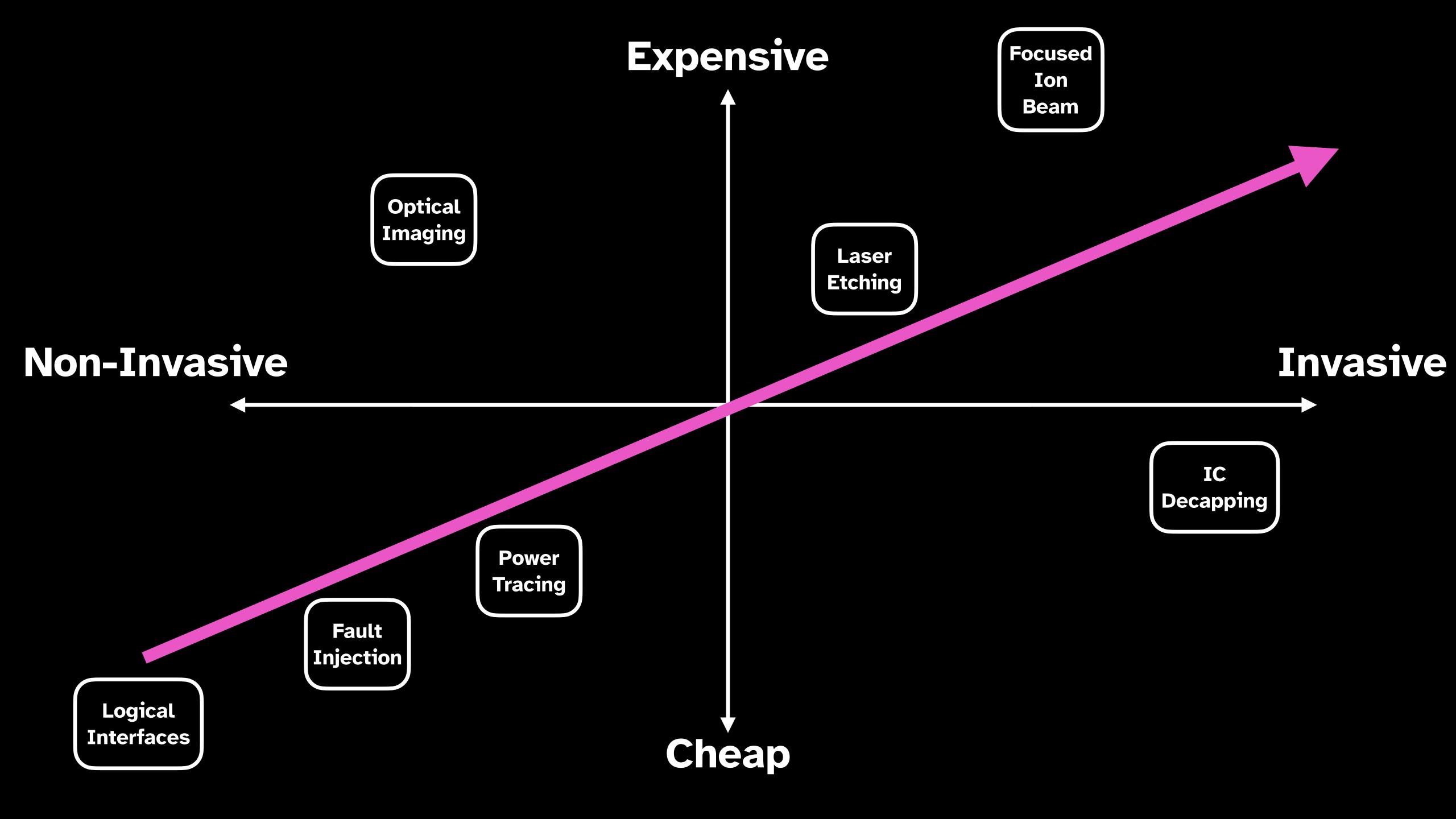
Inject new signals

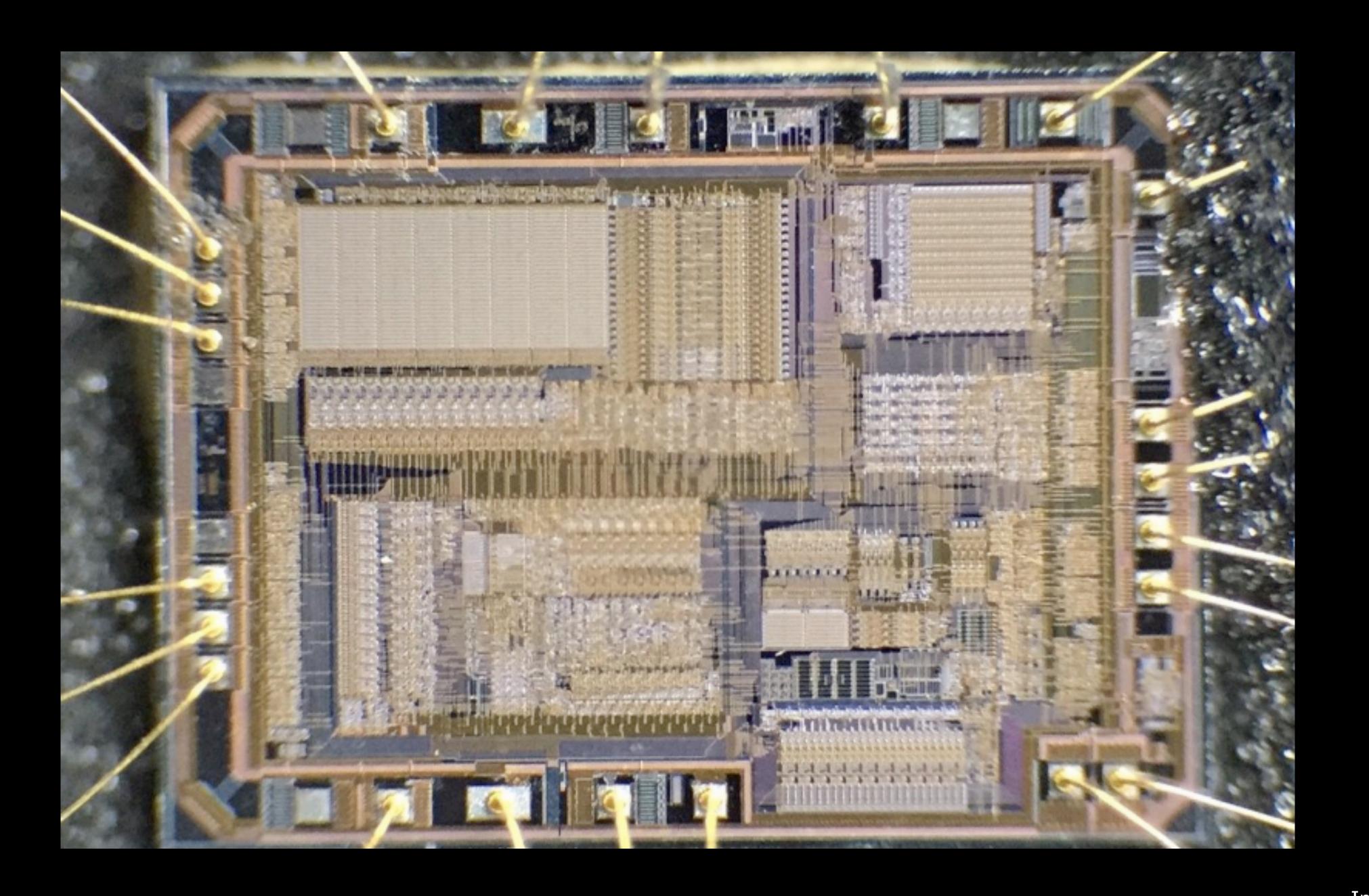
Modify existing signals in new ways

Passive

No modification of signals

Only observe regular operation





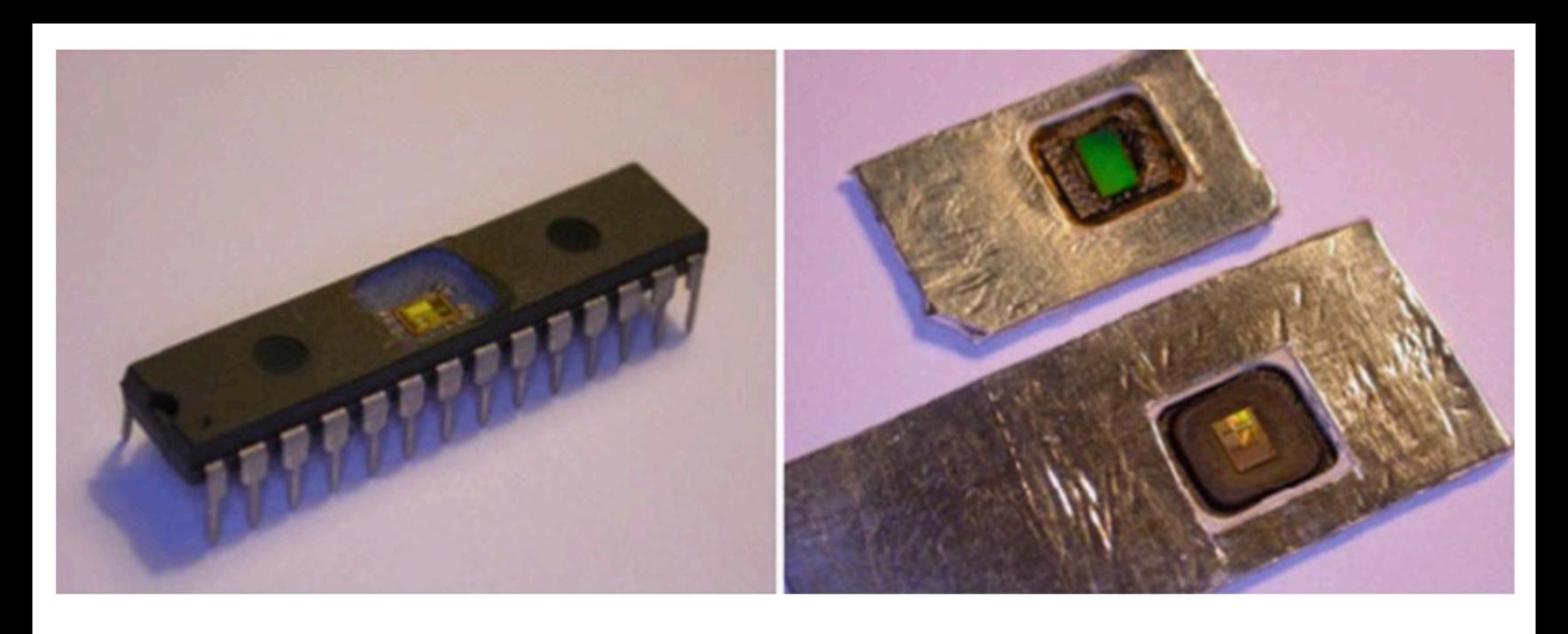


Fig. 7.3 Decapsulated chips



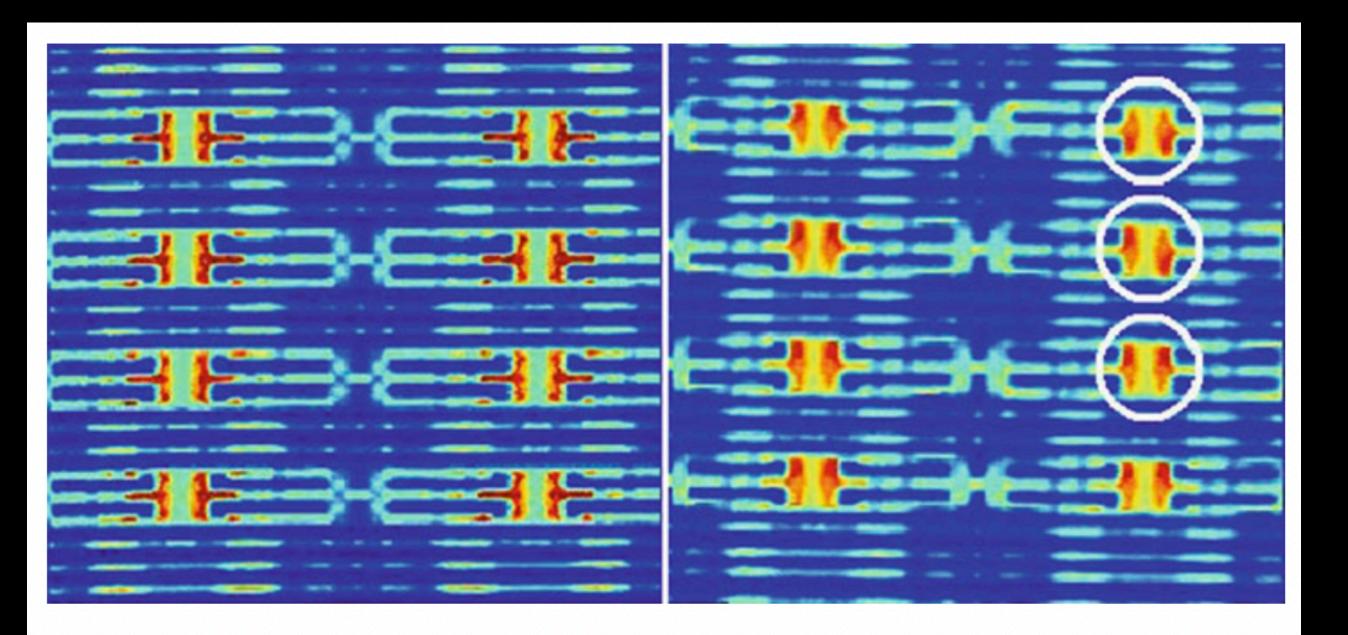


Fig. 7.6 Laser scan of unpowered and powered-up SRAM in PIC16F84 microcontroller

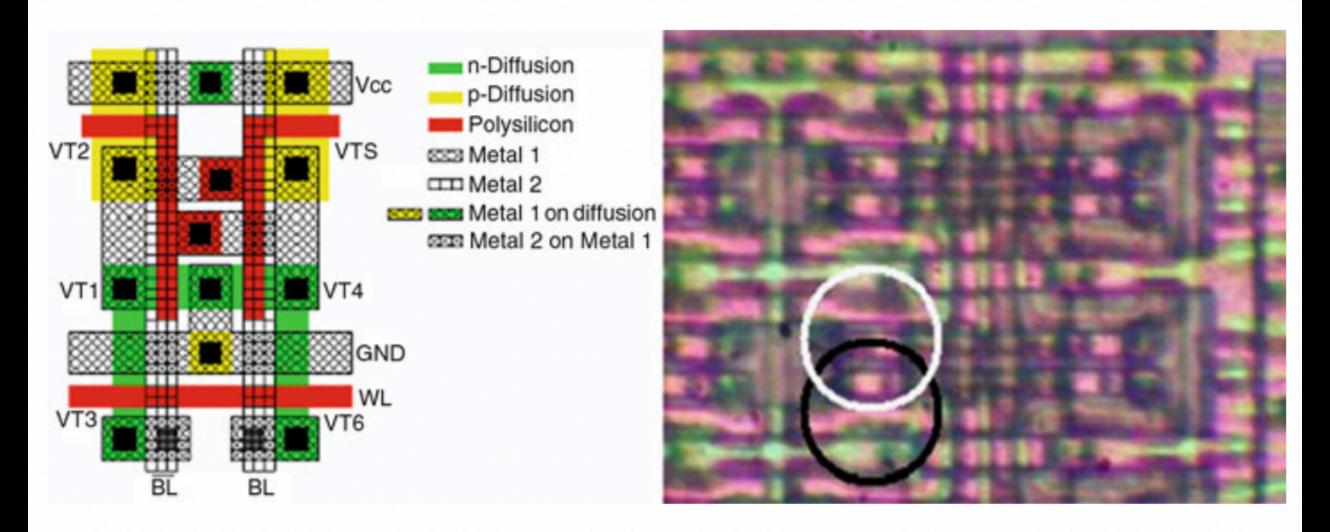


Fig. 7.7 Layout of SRAM cell and SRAM area in PIC16F84 microcontroller

4 Attacks

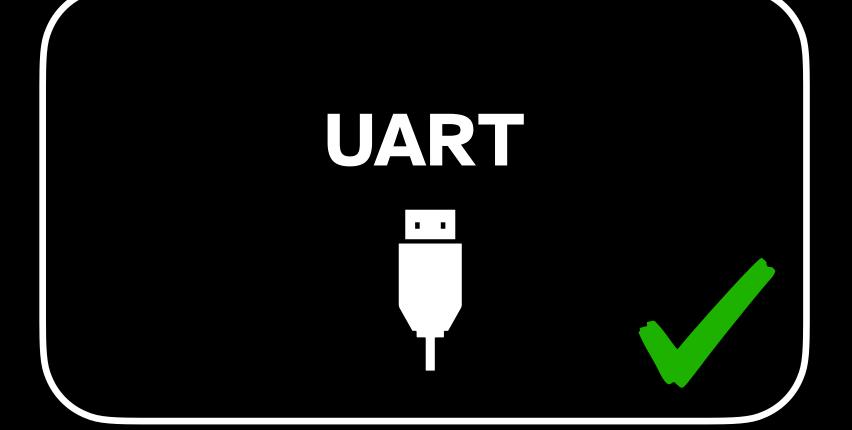
in this class.

Active Fault Injection

Passive

Power Analysis





Timing Analysis



Fault Injection

Chips have strict operating conditions

iectricai	characteristics	STM32F765xx STM32F767xx STM	132F76	8AX S	5 I M32F	/69X
Symbol	Table 17. Gener Parameter	ral operating conditions (continue Conditions ⁽¹⁾	d) Min	Тур	Max	Uni
V ₁₂	Regulator ON: 1.2 V internal voltage on V _{CAP_1} /V _{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 144 MHz HCLK max frequency	1.08	1.14	1.20	_ V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 180 MHz HCLK max frequency with over-drive OFF or 216 MHz with over-drive ON	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V _{CAP_1} /V _{CAP_2} pins ⁽⁷⁾	Max frequency 144 MHz	1.10	1.14	1.20	
		Max frequency 168MHz	1.20	1.26	1.32	
		Max frequency 180 MHz	1.26	1.32	1.38	
V _{IN}	Input voltage on RST and FT pins ⁽⁸⁾	2 V ≤V _{DD} ≤3.6 V	- 0.3	-	5.5	
		V _{DD} ≤2 V	- 0.3	-	5.2	
	Input voltage on TTa pins	-	- 0.3	-	V _{DDA} + 0.3	
	Input voltage on BOOT pin	-	0	-	9	
P _D	Power dissipation at $T_A = 85$ °C for suffix 6 or $T_A = 105$ °C for suffix $7^{(9)}$	LQFP100	-	-	465	mW
		WLCSP180	-	-	641	
		LQFP144	-	-	500	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
		TFBGA100	-	-	552	
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	- 40	-	85	- °C
		Low power dissipation ⁽¹⁰⁾	- 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	- 40	-	105	- °C
		Low power dissipation ⁽¹⁰⁾	- 40	-	125	
TJ	Junction temperature range	6 suffix version	- 40	-	105	°C
		7 suffix version	- 40	-	125	`





Chips have strict operating conditions

Intentionally inject outof-specification inputs to (hopefully) break the chip

lectrical	characteristics	STM32F765xx STM32F767xx STM	132F76	8Ax S	STM32F	769xx					
Table 17. General operating conditions (continued)											
Symbol	Parameter	Conditions ⁽¹⁾	Min	Тур	Max	Unit					
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		LQFP176	-	-	526						
		UFBGA176	-	-	513						
		LQFP208	-	-	1053						
		TFBGA216	-	-	690						
		TFBGA100	-	-	552						
Та	Ambient temperature for 6 suffix version	Maximum power dissipation	- 40	-	85	°C					
		Low power dissipation ⁽¹⁰⁾	- 40	-	105						
	Ambient temperature for 7 suffix version	Maximum power dissipation	- 40	-	105	- °C					
		Low power dissipation ⁽¹⁰⁾	- 40	-	125						
TJ	Junction temperature range	6 suffix version	- 40	-	105						
		7 suffix version	- 40	-	125	- °C					

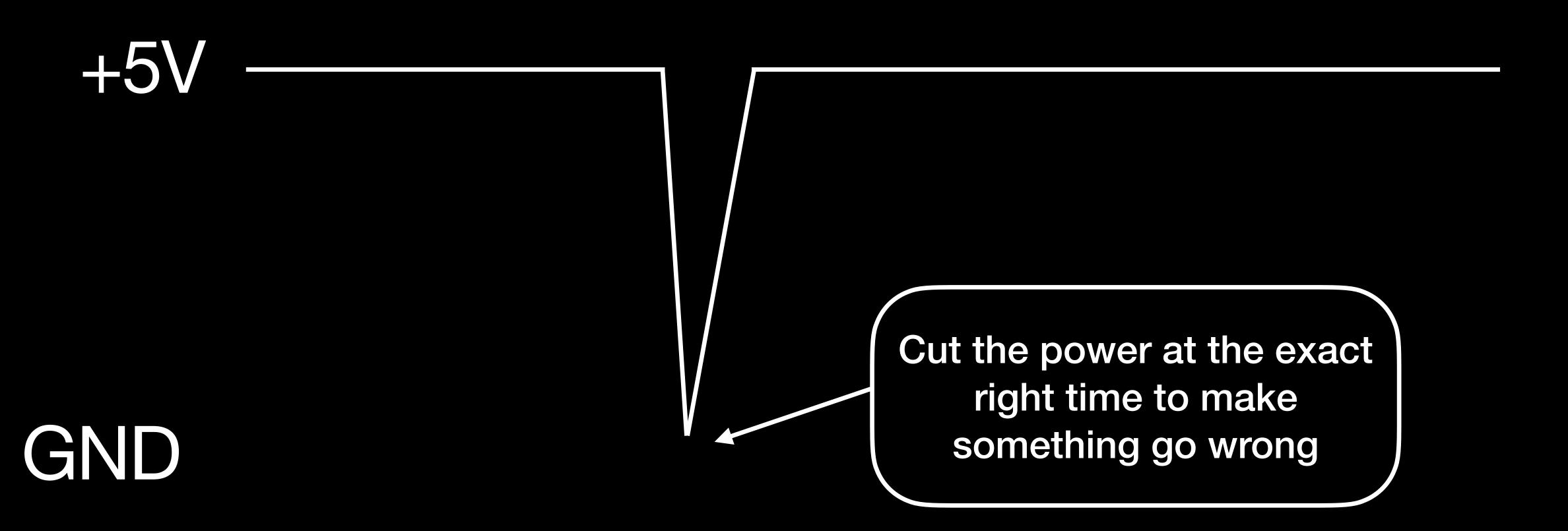
Normal Input Voltage (Vcc)

+5V

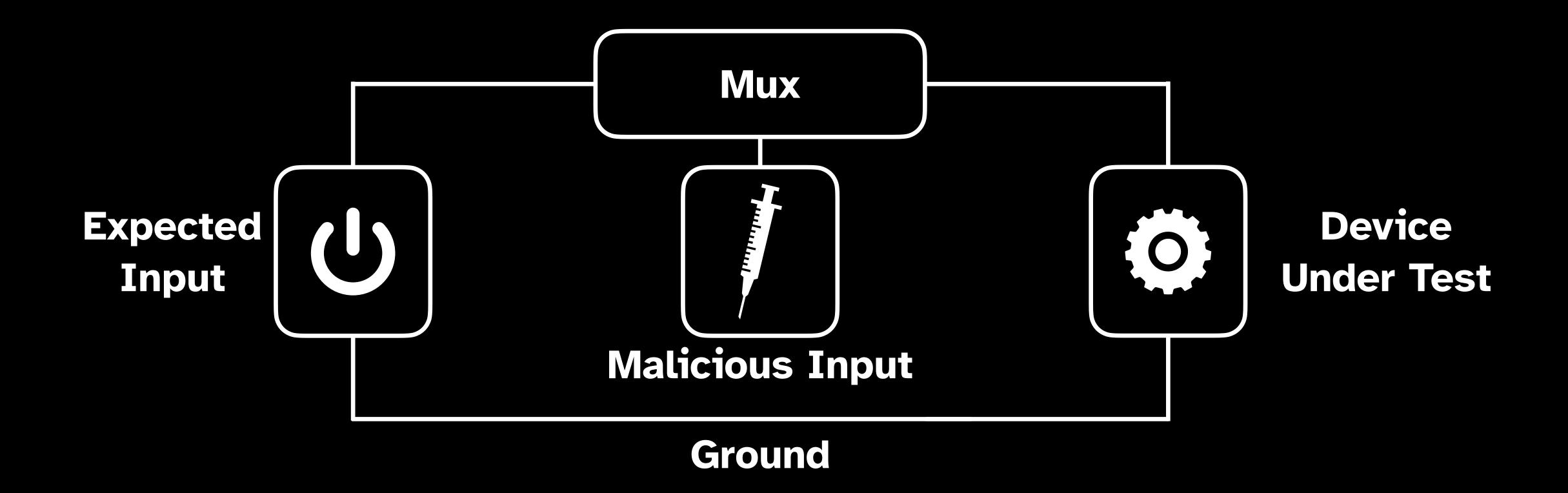
GND



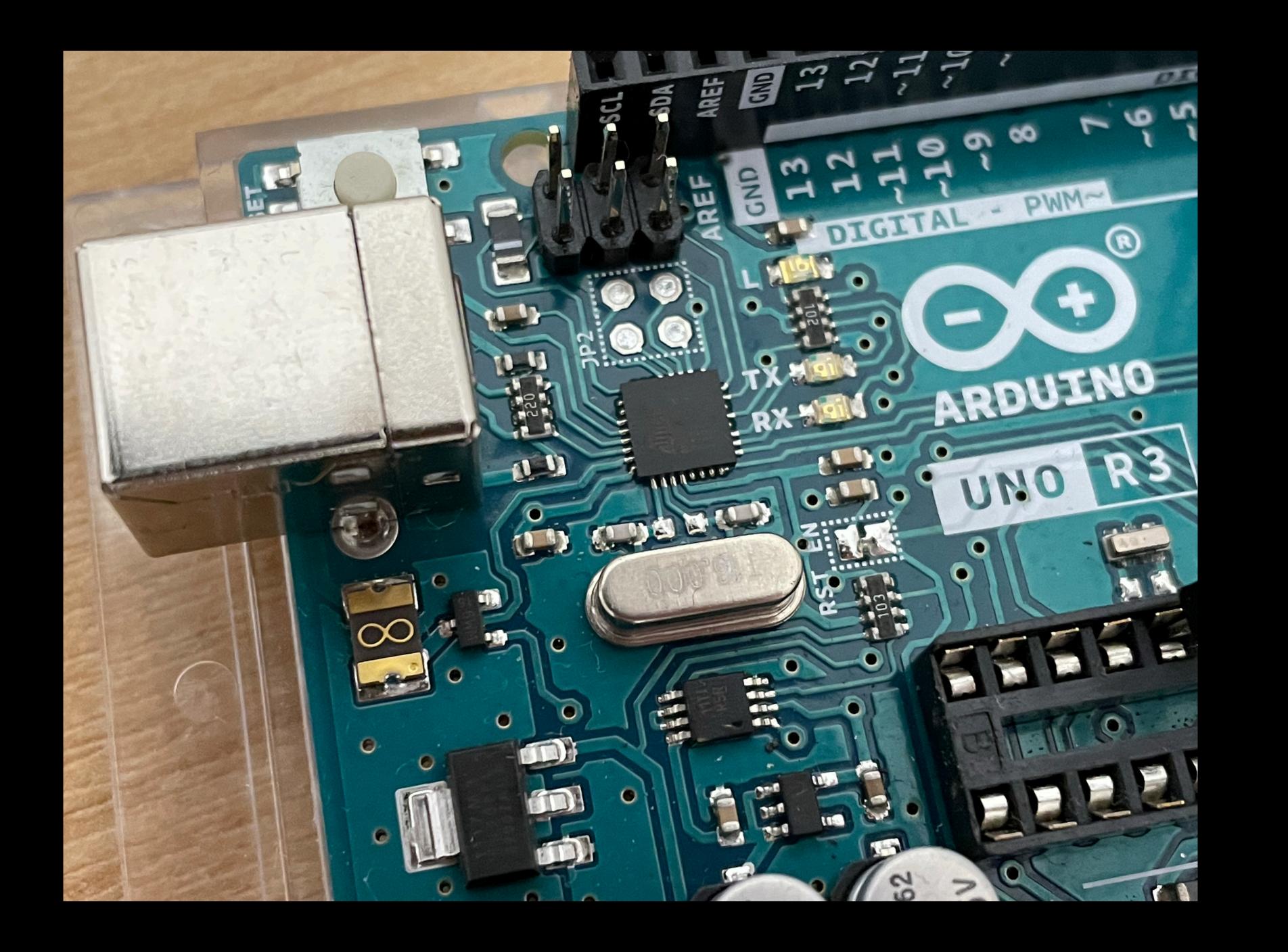
Voltage Glitching

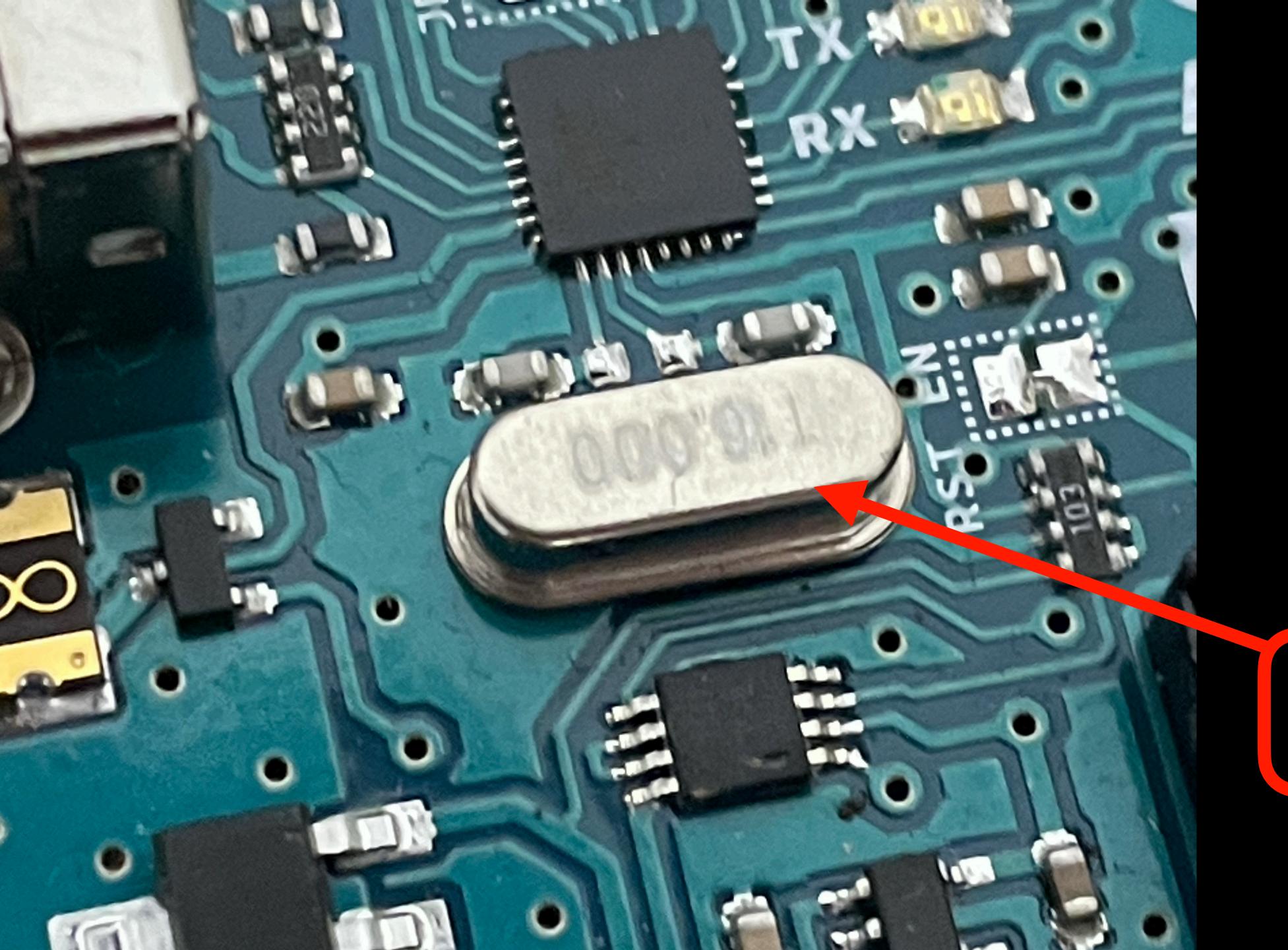








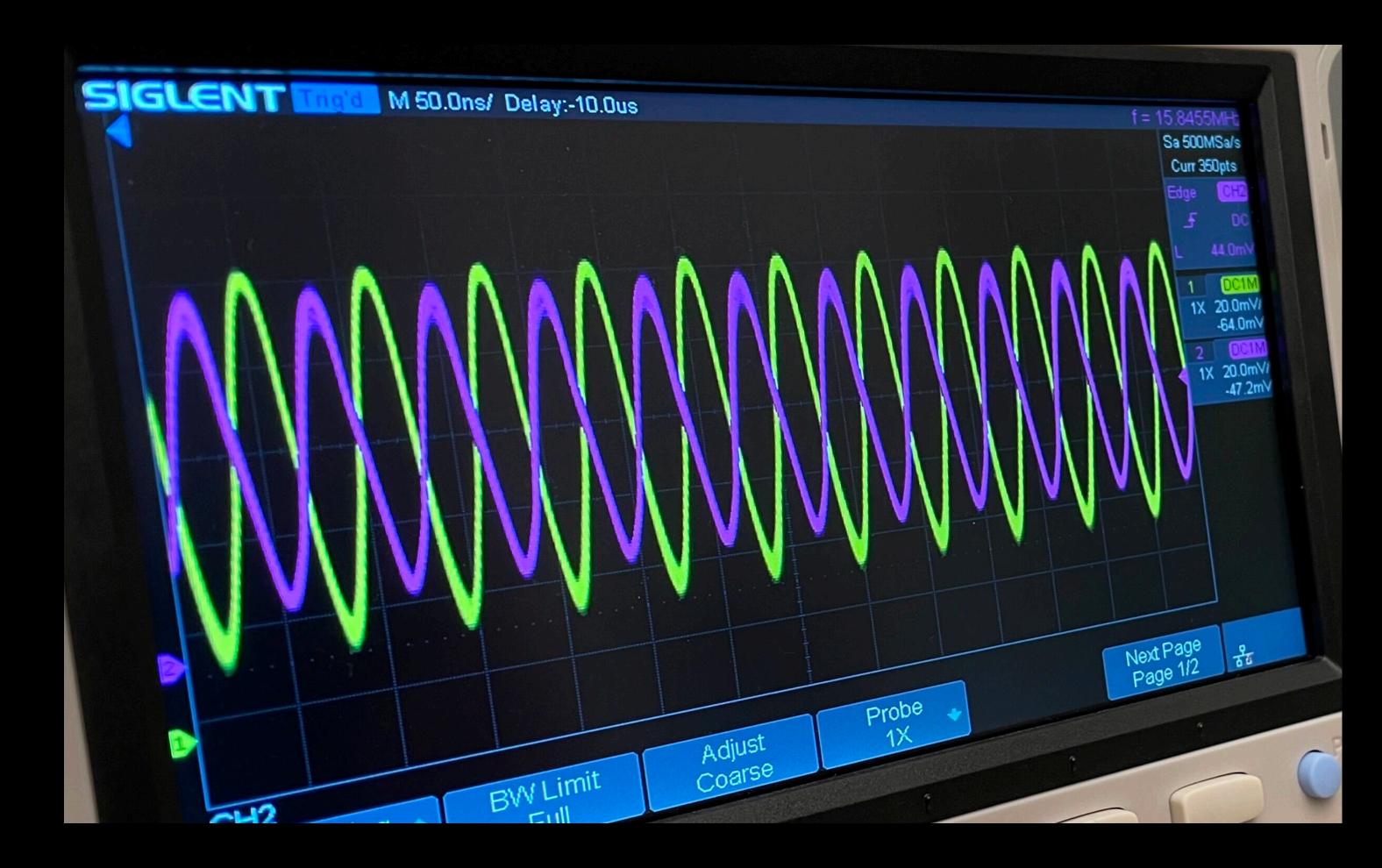




Crystal Oscillator

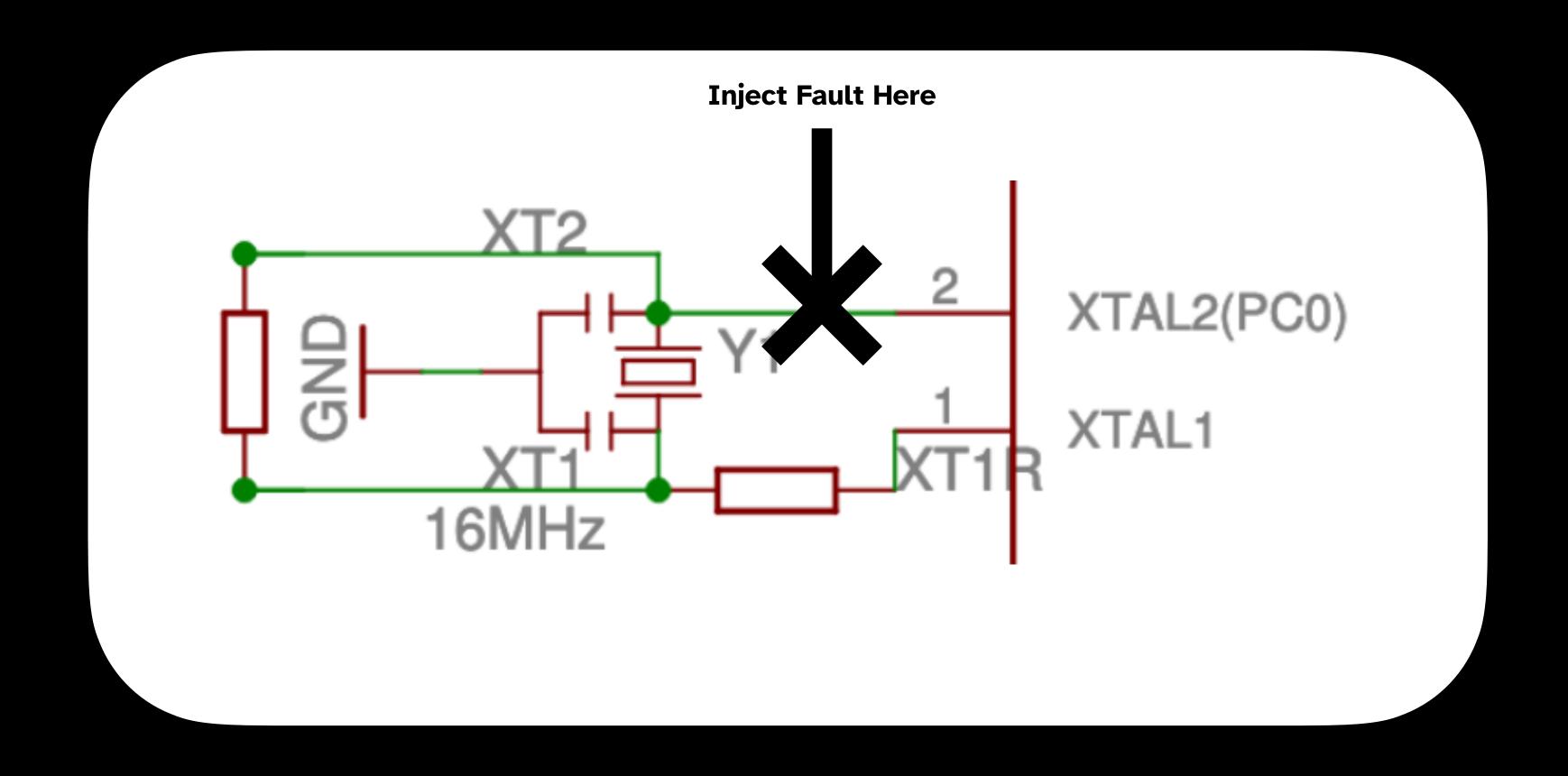
Clock Glitching

Oscillator Cap Cap Ground

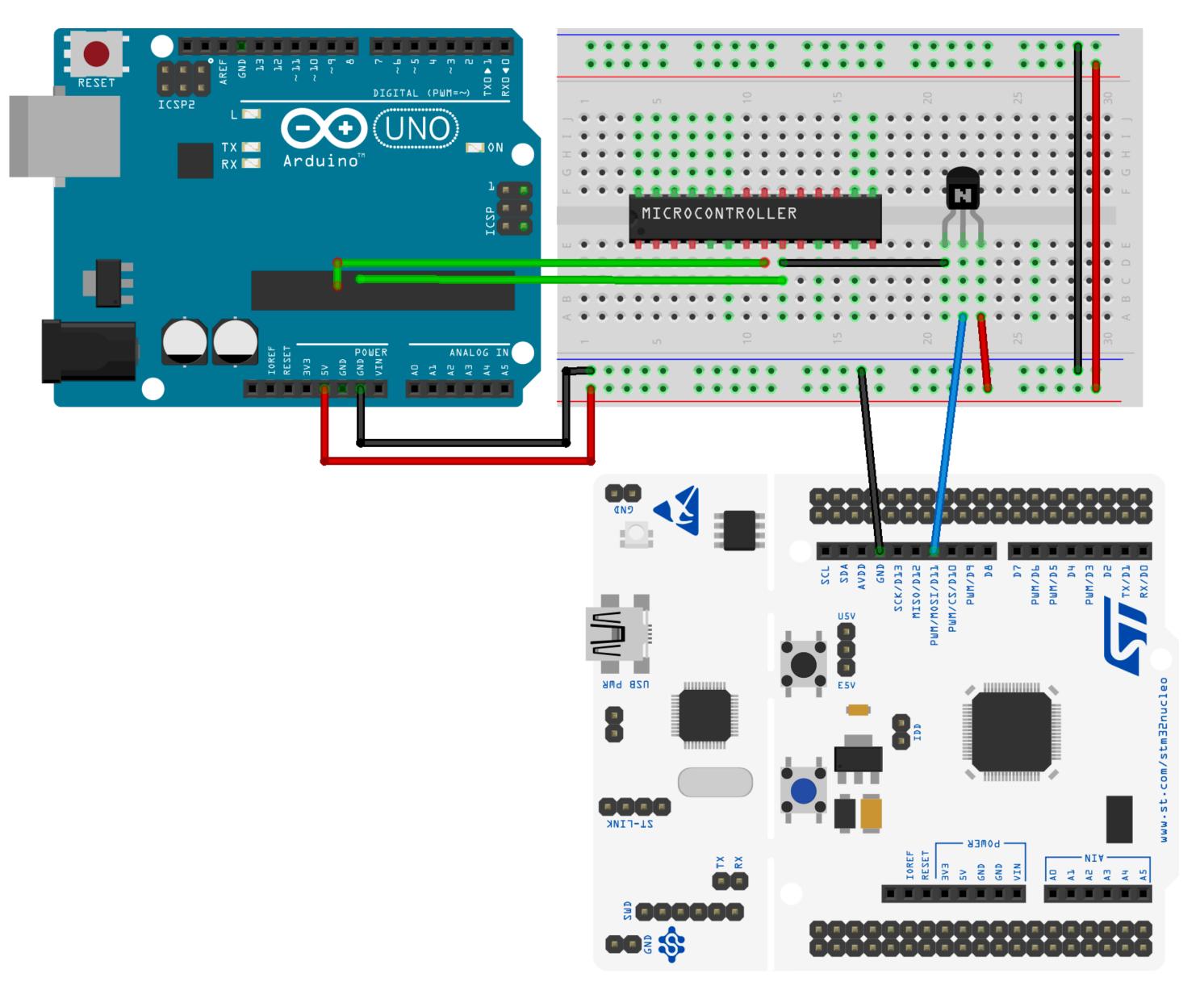




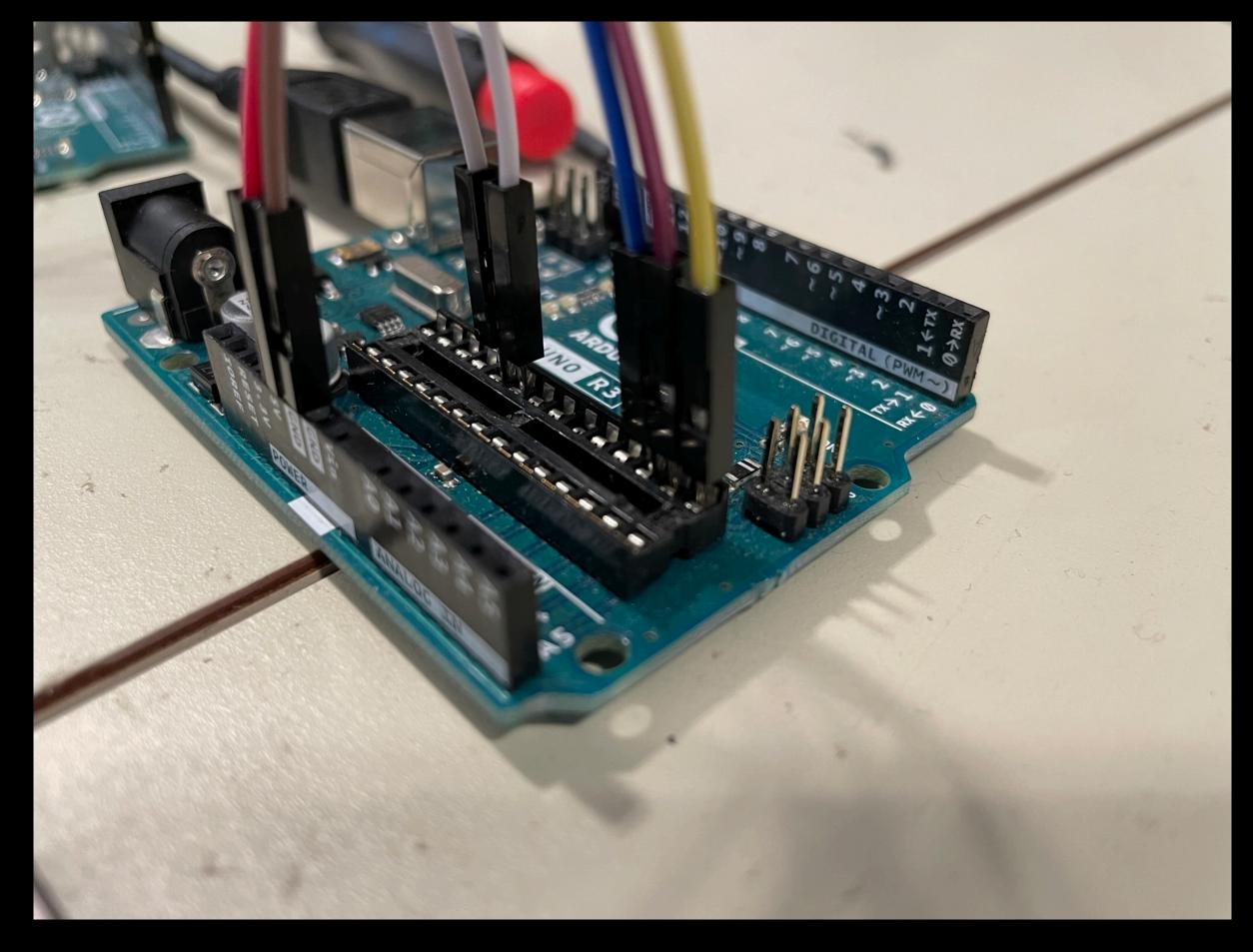
Crystal Oscillator

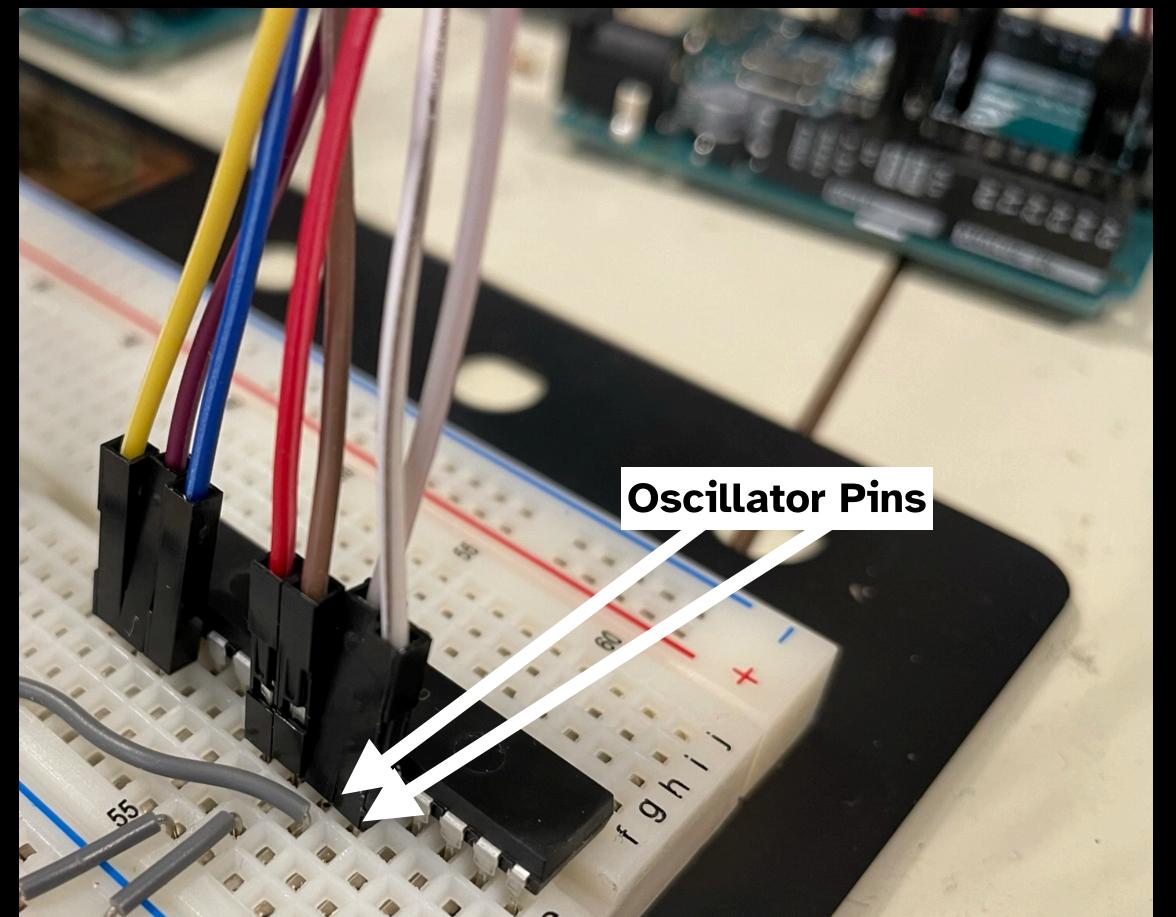


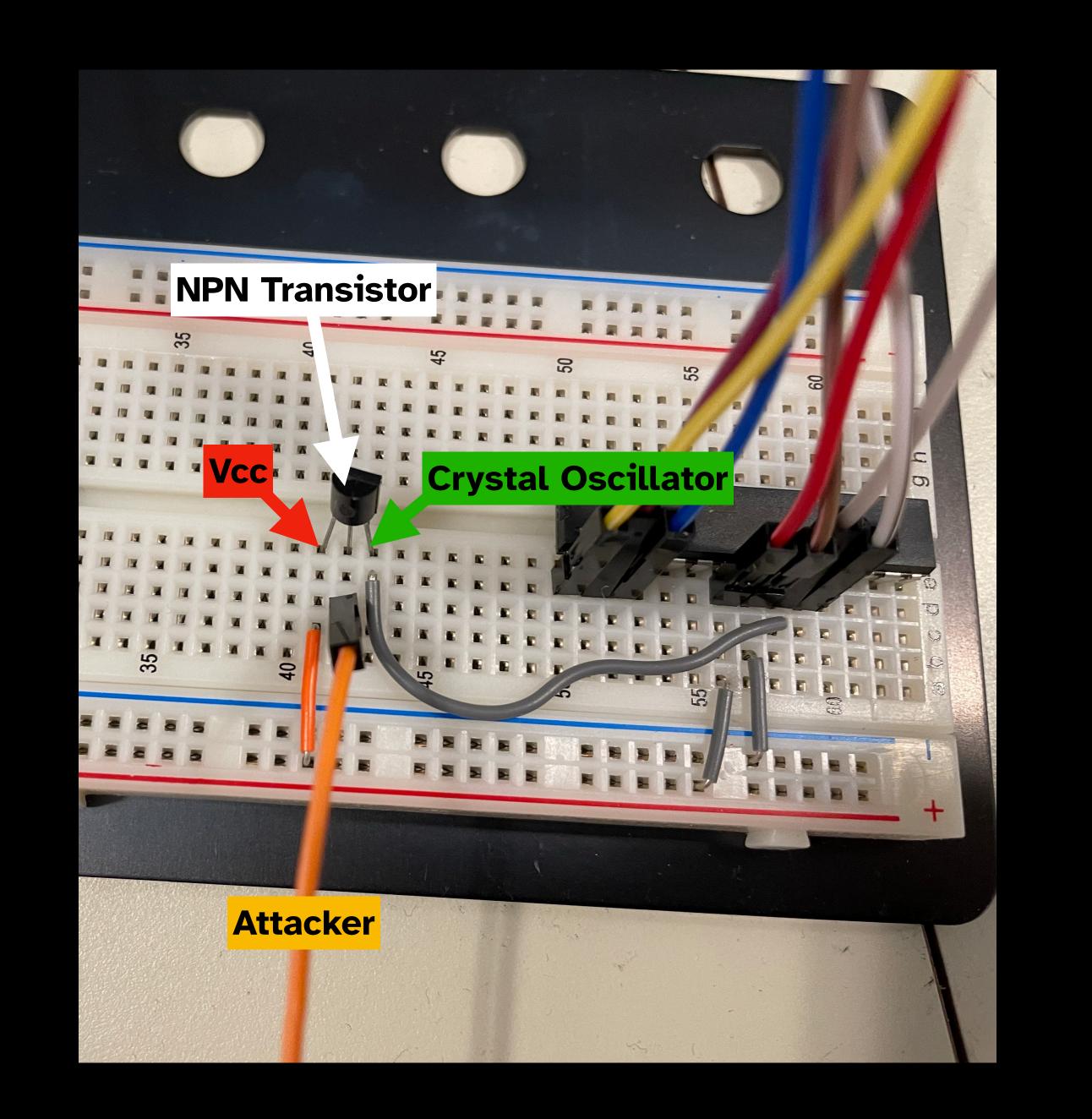


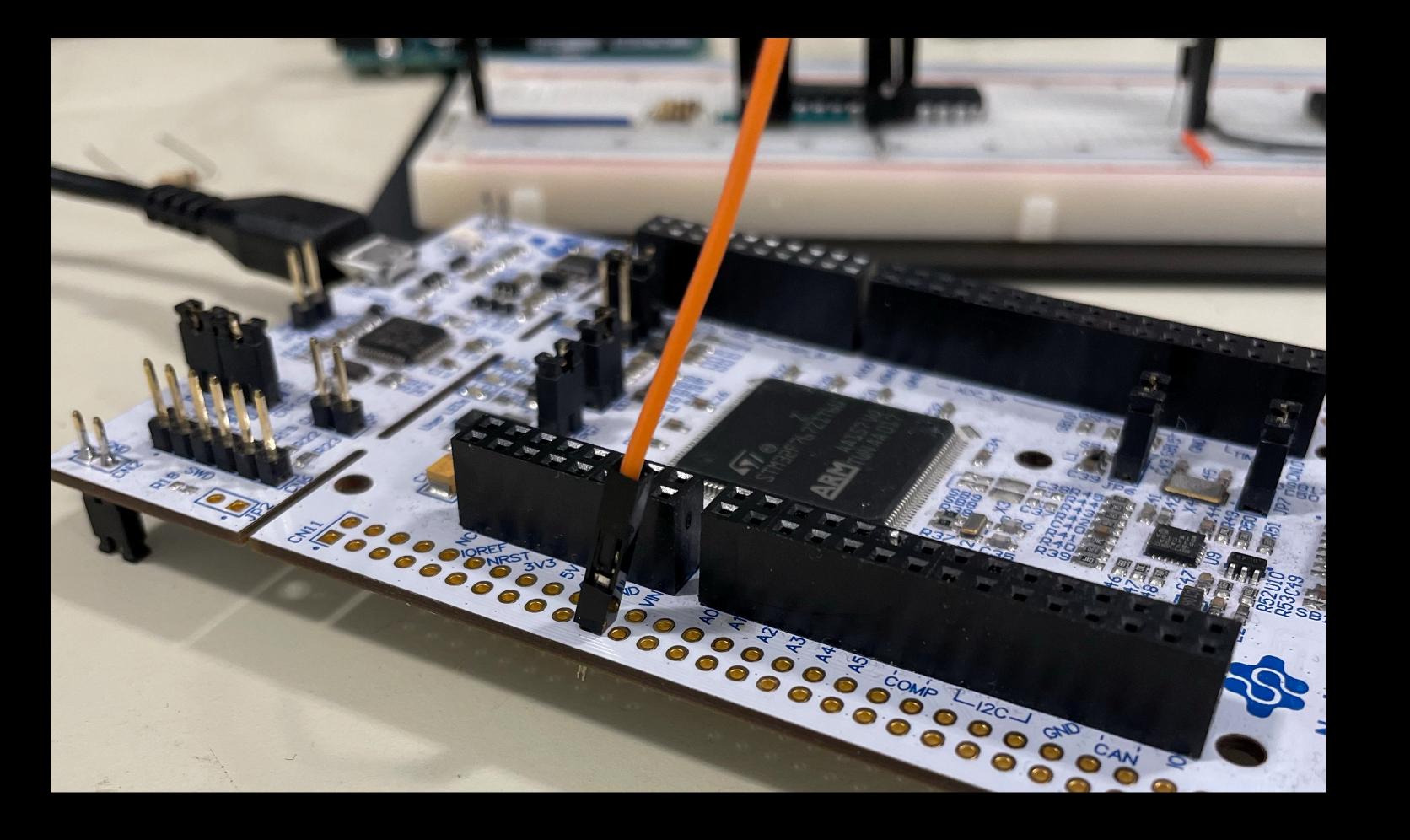


fritzing









Inject Fault here

```
while(1 == 1) {
    print("Locked! %d", iter);
    iter++;
}
print("MIT{flag}");
```

"What if we intentionally violate the chip's expected operating conditions?"

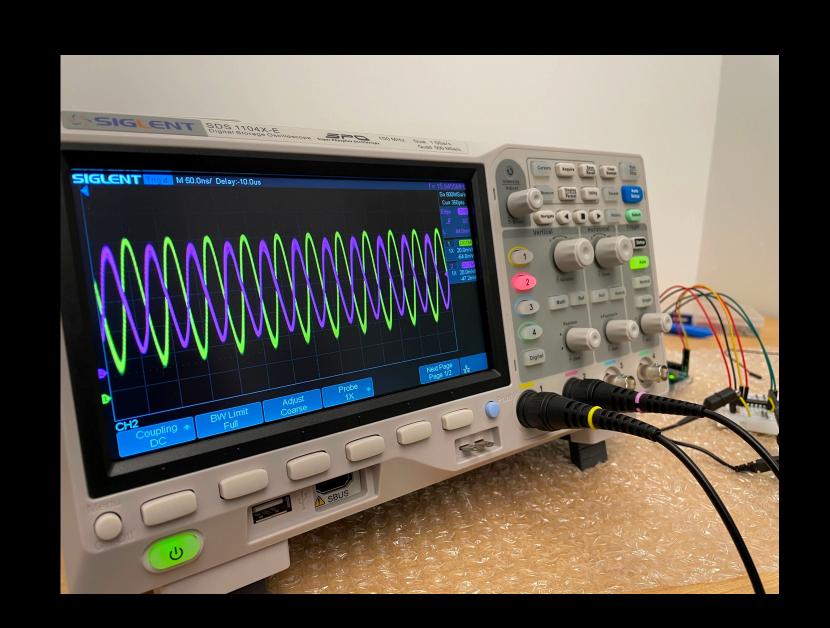


Cheap

Affordable

Crazy Expensive

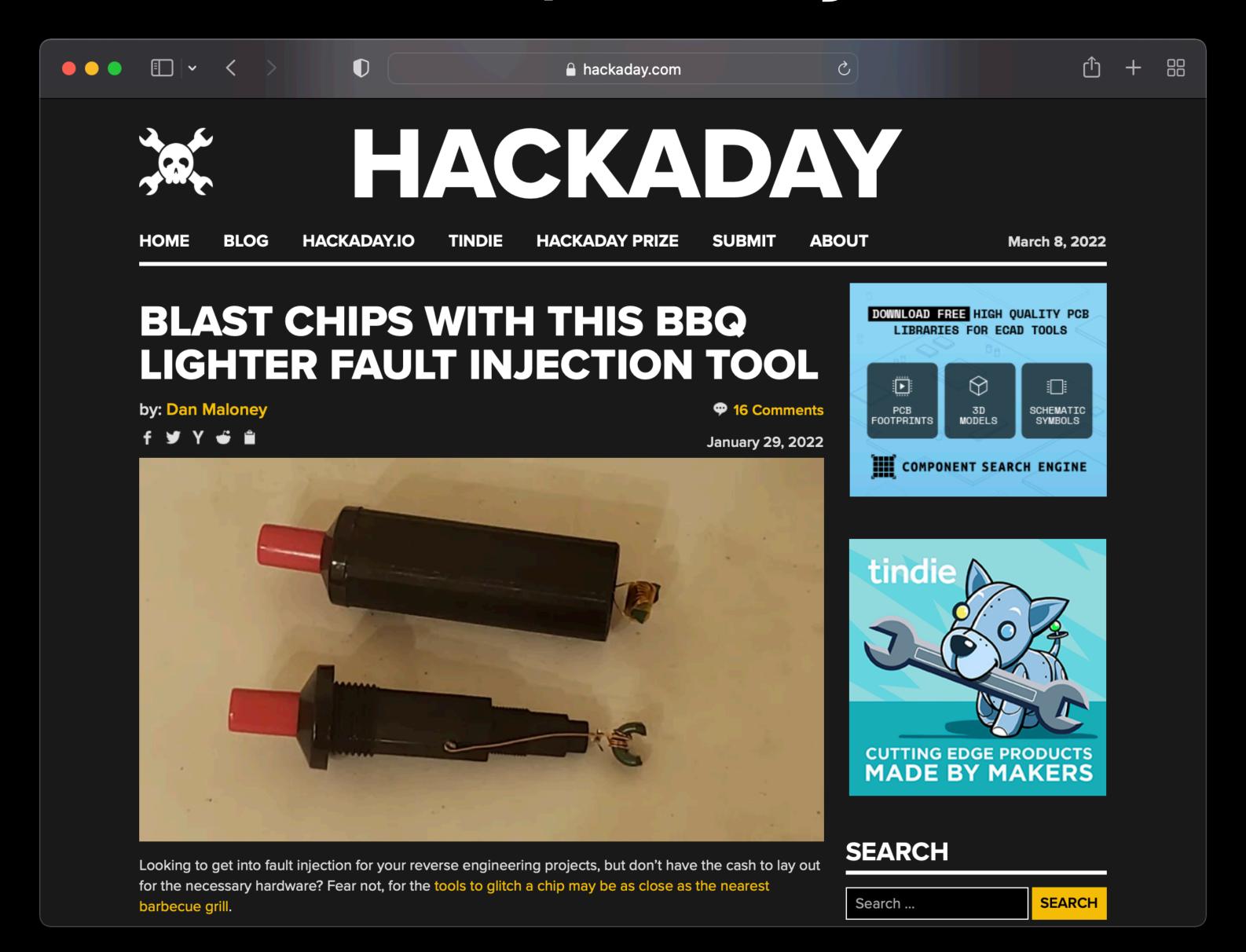




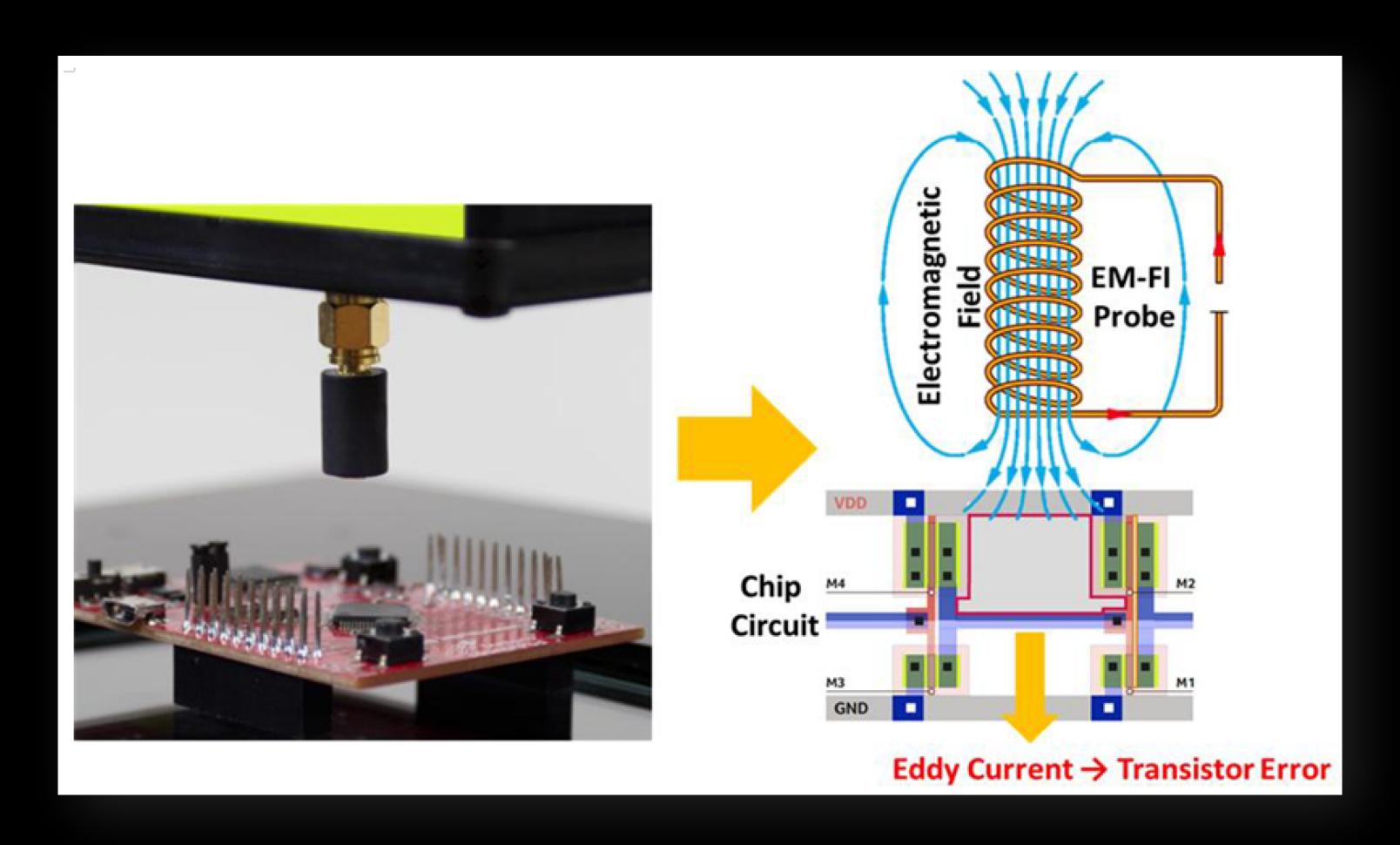




Yes, Really



EM or Photonic Signals Work, Too.



Lim et al. Novel Fault Injection Attack without Artificial Trigger. Applied Science



Notable Examples



158K subscribers



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So, why does that work?

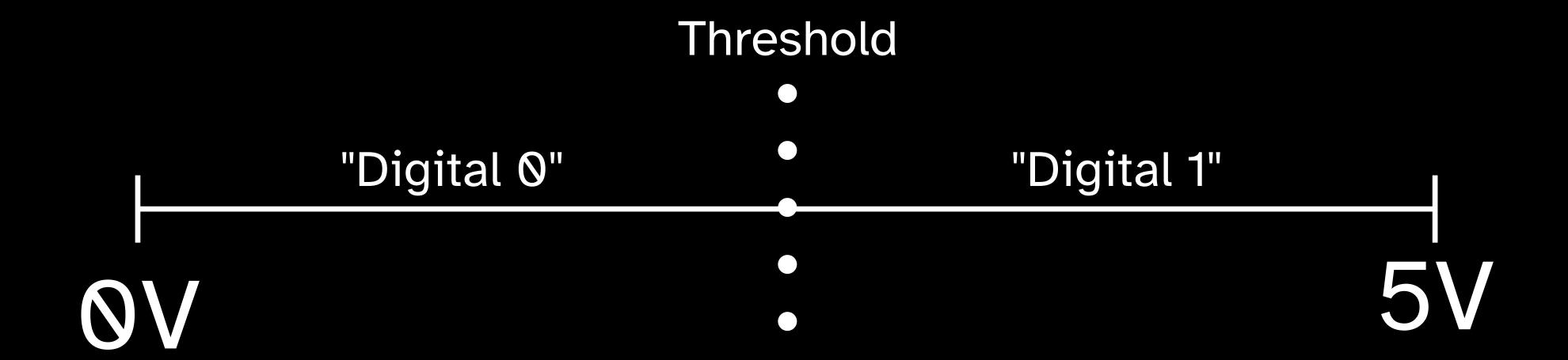


Representing 0s and 1s





Representing 0s and 1s



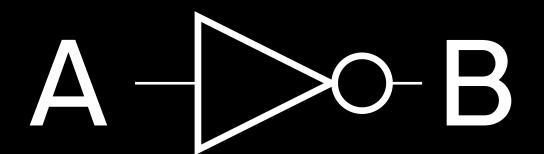


Representing 0s and 1s

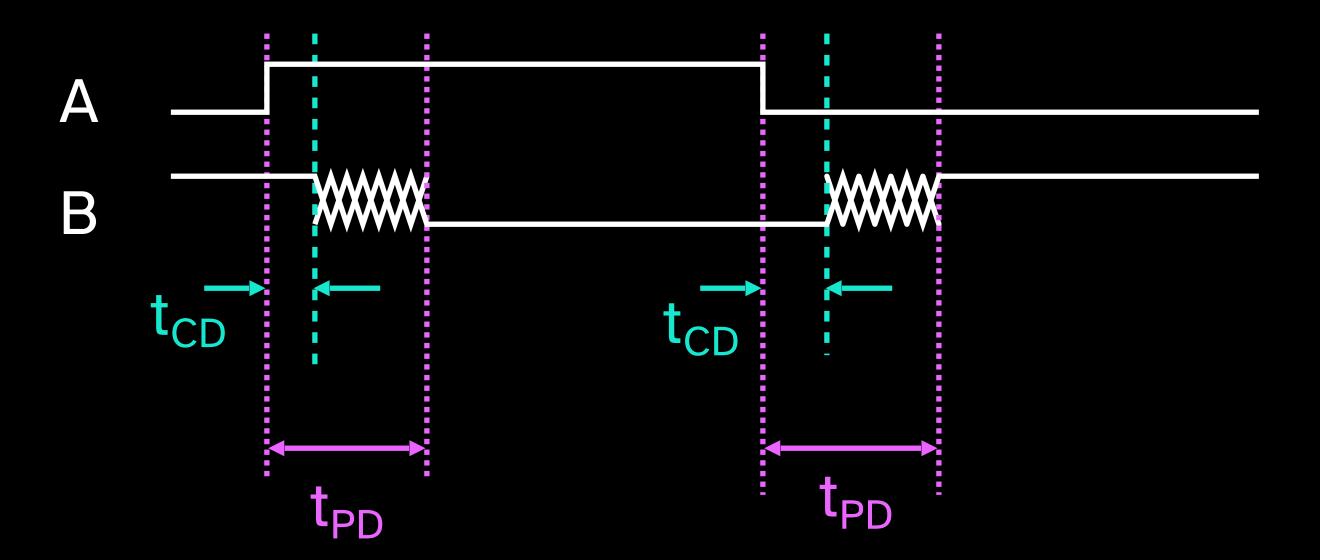




Real-World Circuits Take Time



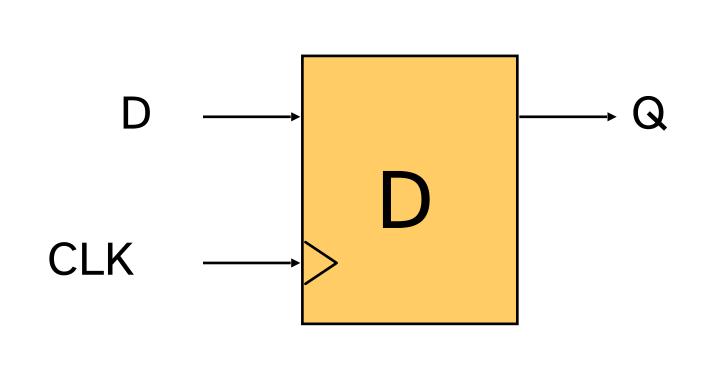
A	В
0	1
1	0

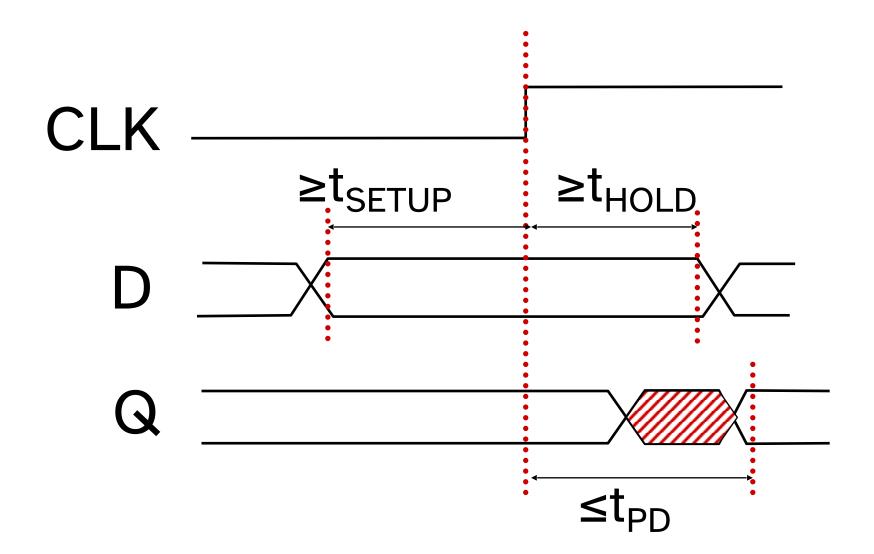


ton Propagation Delay
ton Contamination Delay



D Flip-Flop Timing (CLK Edge Trigger)

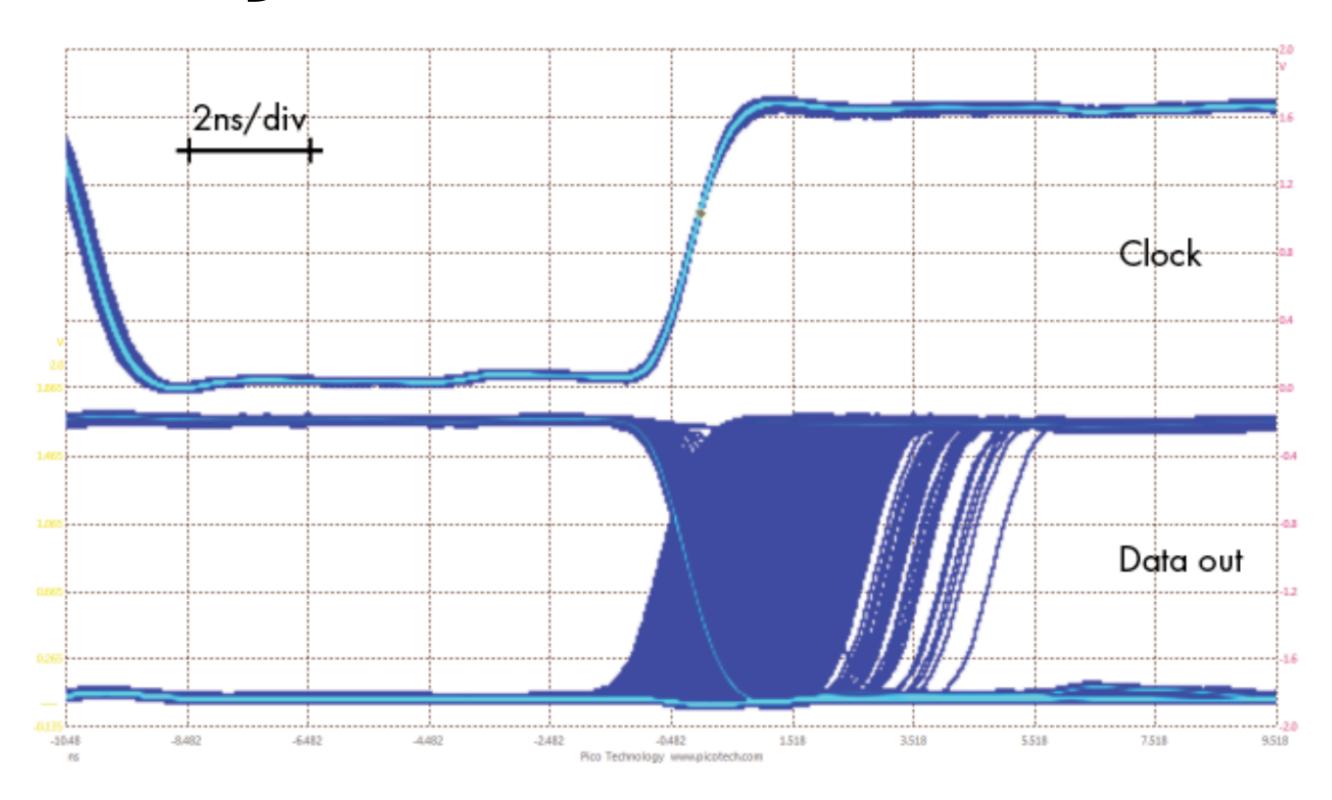




- Flip-flop input D should not change around the rising edge of the clock to avoid metastability
- Formally, D should be a stable and valid digital value:
 - For at least t_{SETUP} before the rising edge of the clock
 - For at least t_{HOLD} after the rising edge of the clock
- Violating the timing constraints leaves the circuit in a metastability state. A contaminated value will be loaded into the register.



Metastability

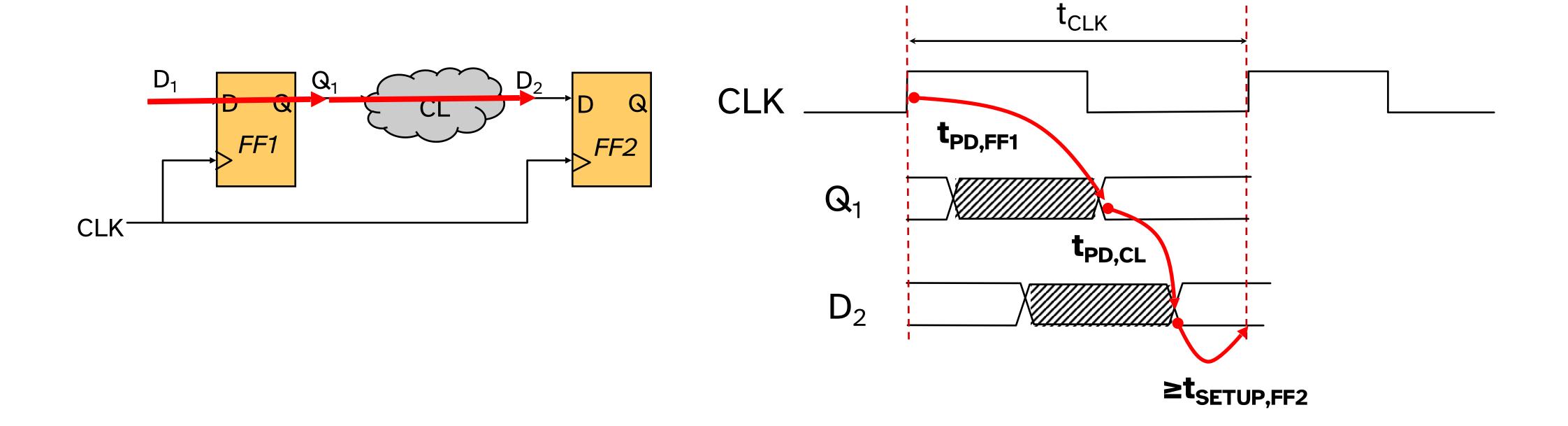


<u>Figure 5-7</u>: Metastable data output from shifting the clock edge to cause timing violations (low-voltage operation)

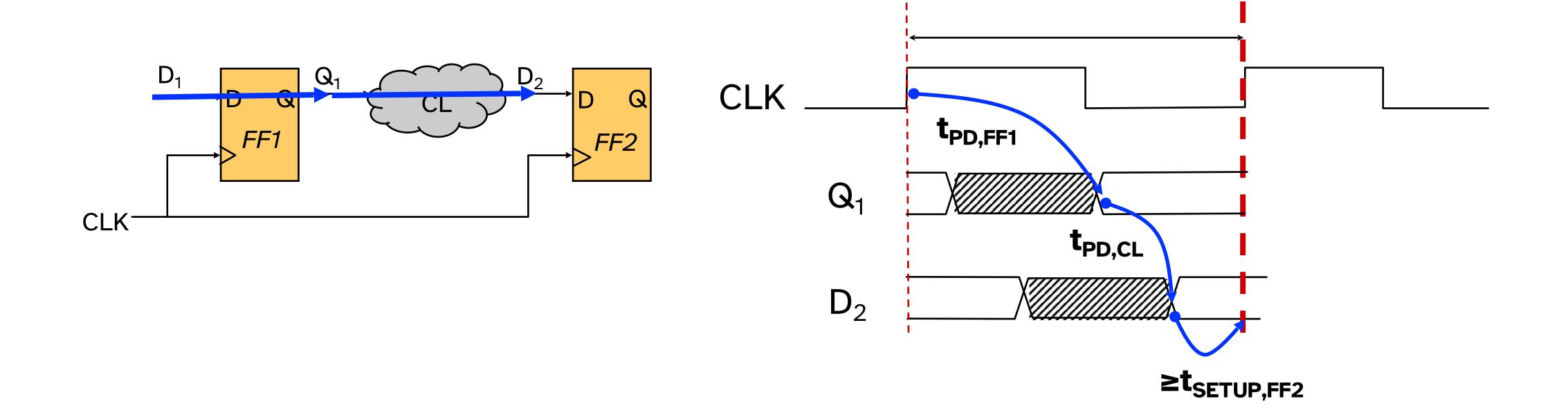
Colin O'Flynn. The Hardware Hacking Handbook. Chapter 5 Figure 5-8. No Starch Press.



Sequential Circuit Timing (Setup Time)



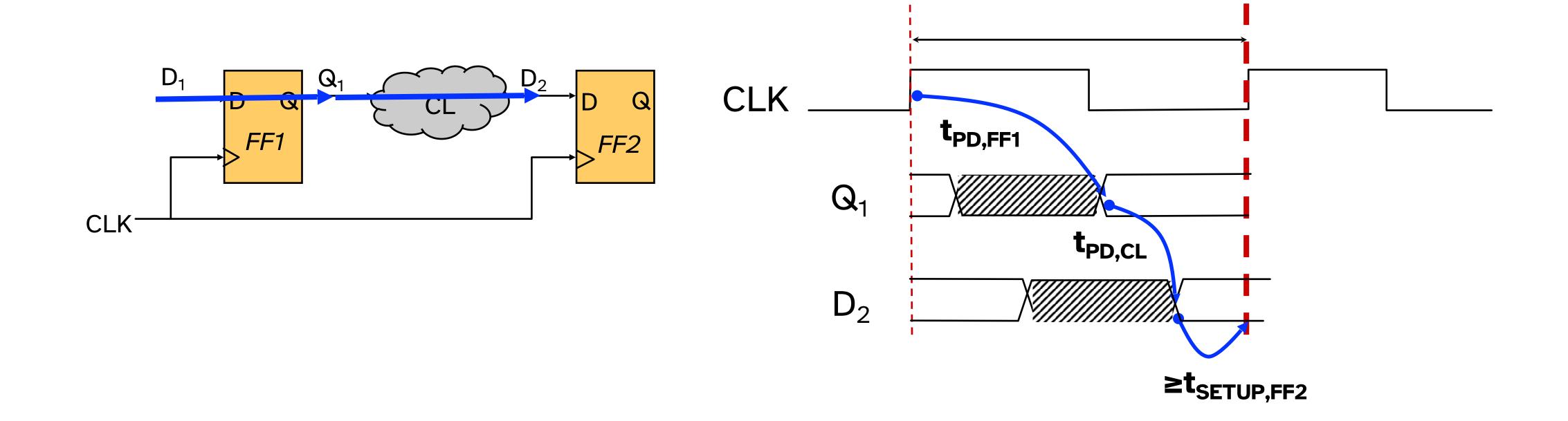
Fault Injection Attacks



What if the clock comes earlier?



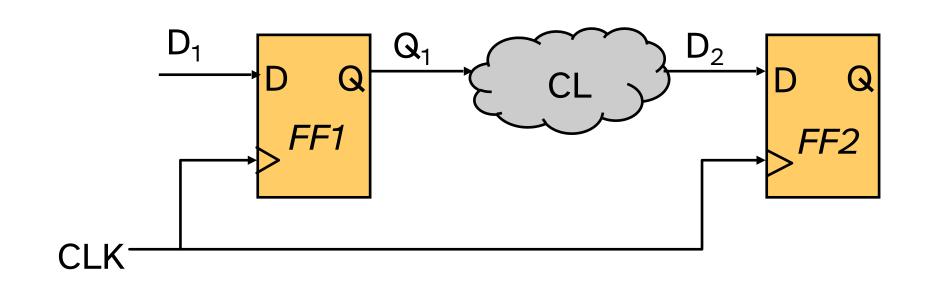
Fault Injection Attacks

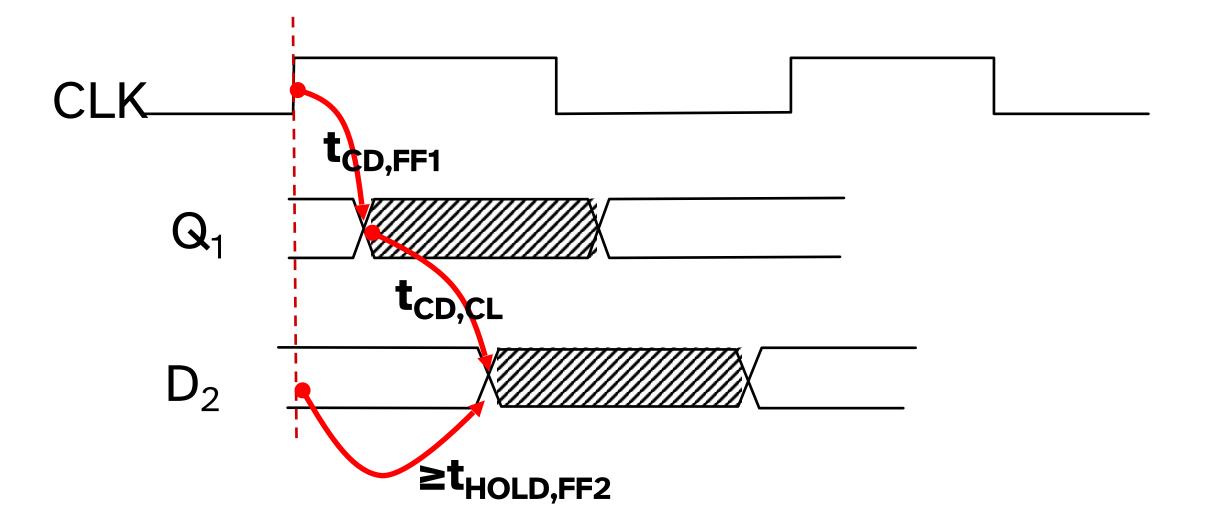


Decreasing the voltage increases propagation delay



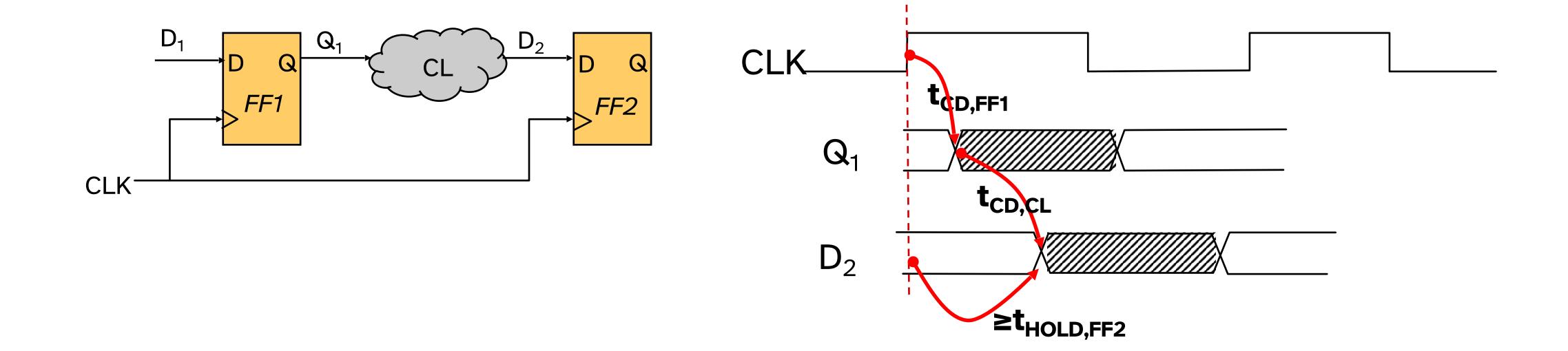
Sequential Circuit Timing (Hold Time)







Voltage Glitching Attacks



Increasing voltage decreases contamination time



Can we stop it?

Mitigations

Redundancy

Think "two cores running the same thing". Can be expensive.

Example: OpenTitan.

Non-Determinism

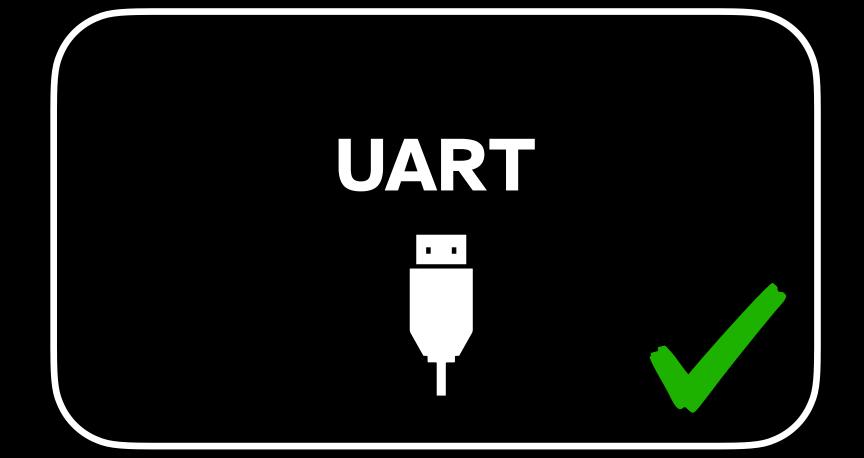
Add randomness to the timing of certain chip operations.

Reduces accuracy of attack.









Timing Analysis

L

Timing Analysis

Spot the Bug

```
bool memcmp (char *buf1, char *buf2, size_t len) {
    for (int i = 0; i < len; i++) {
        if (buf1[i] != buf2[i]) {
             return false;
    return true;
```

Spot the Bug

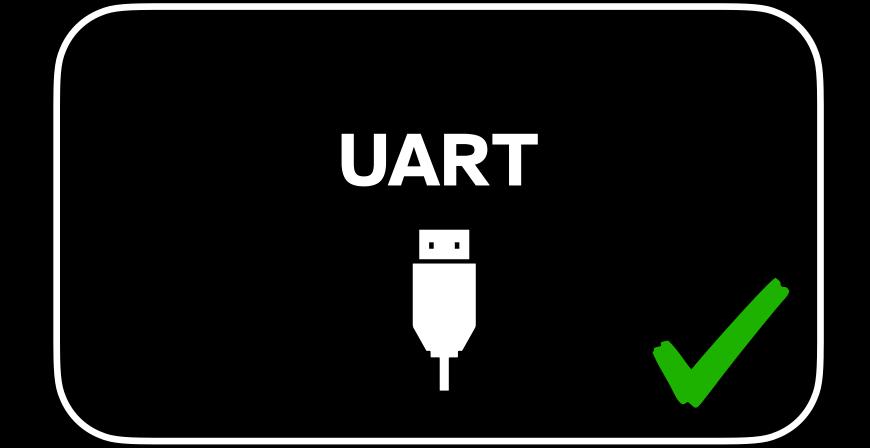
```
bool memcmp (char *buf1, char *buf2, size_t len) {
    for (int i = 0; i < len; i++) {
        if (buf1[i] != buf2[i]) {
             return false;
    return true;
                                  Fatal Flaw
```



No Demo: You will do this in recitation!







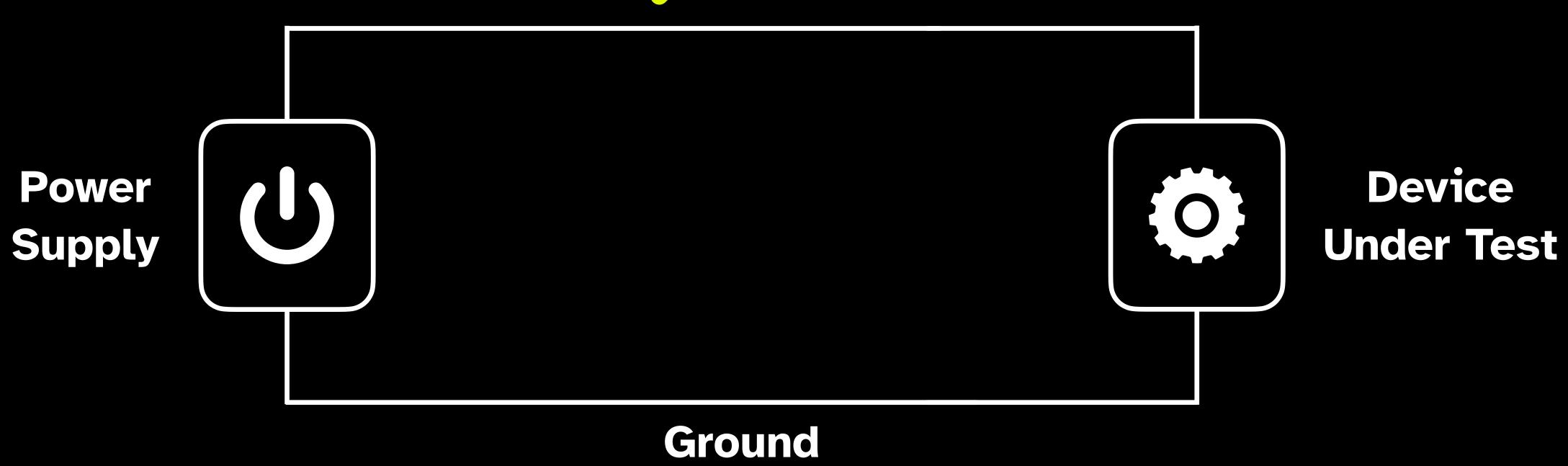


Power Analysis

Power = Voltage x Current



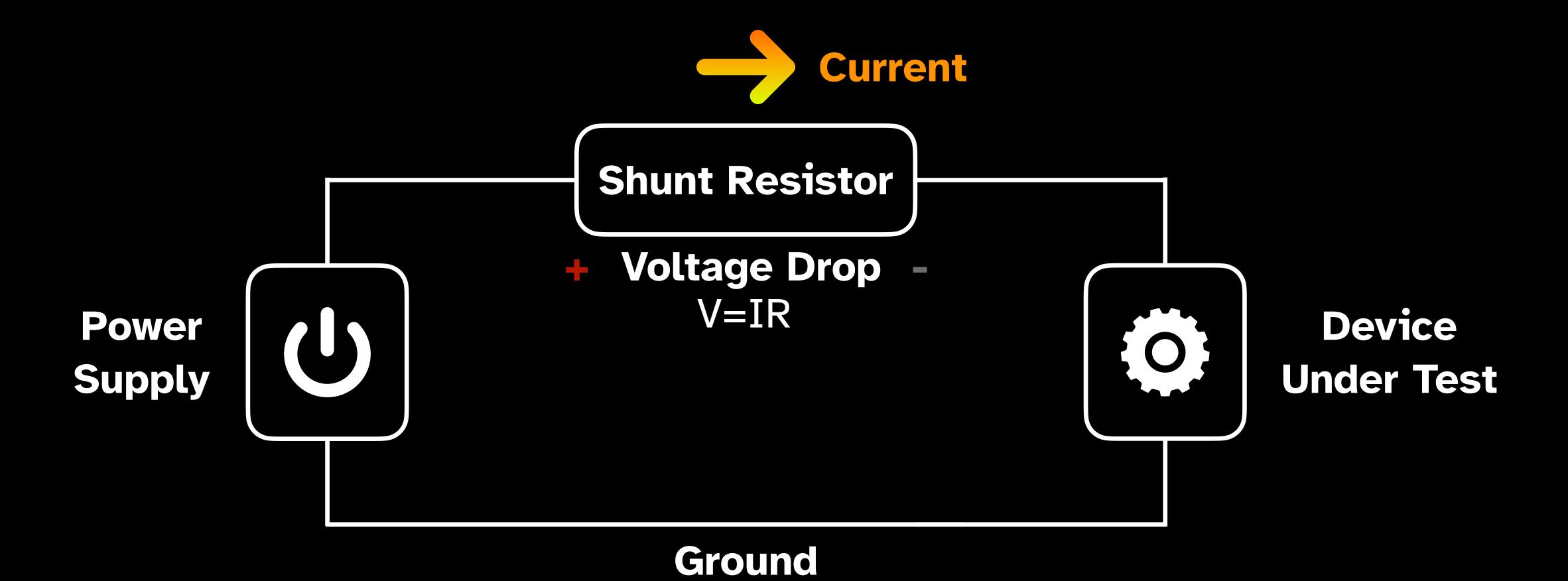






How do you measure current on an oscilloscope?







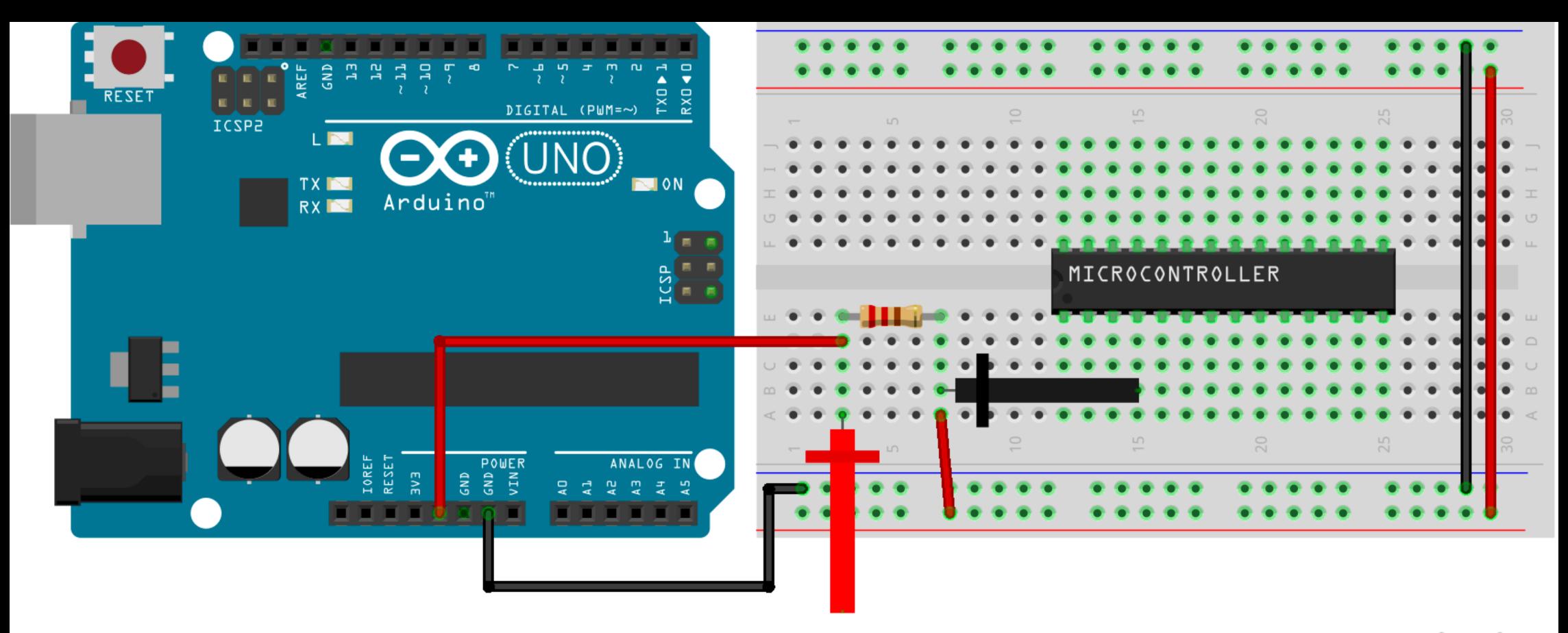
Apply Ohm's Law

Voltage (V) = Current (I) * Resistance (R)

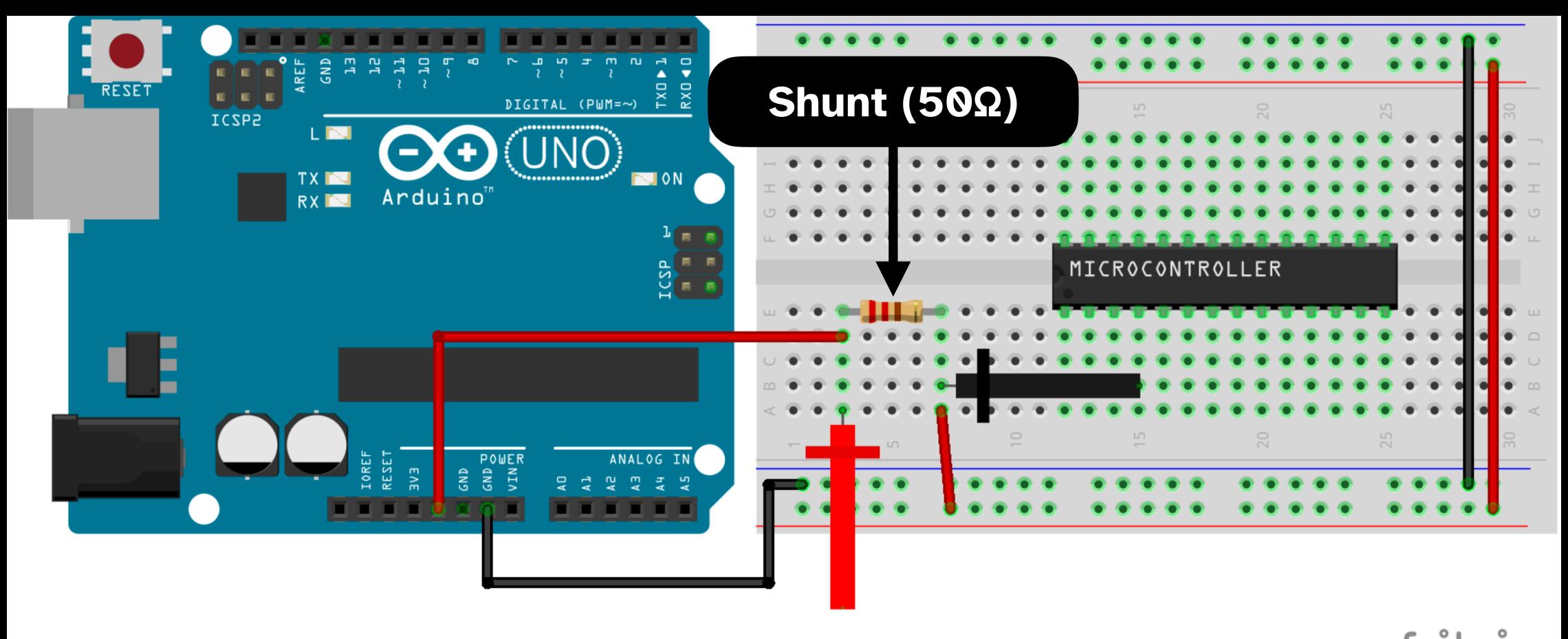
Or in other words,

$$I = V / R$$

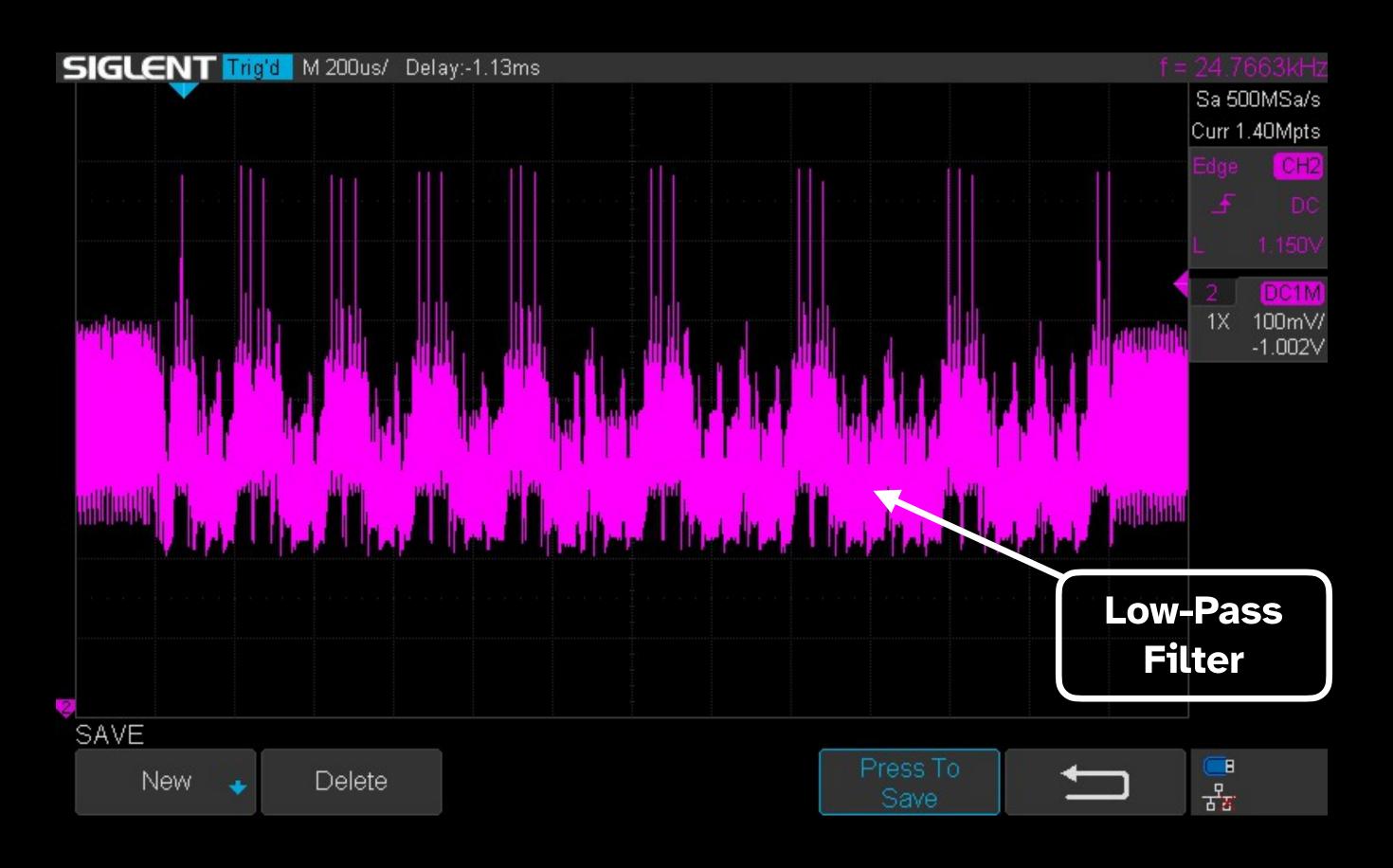




fritzing



fritzino



```
int rsa_modExp(int b, int e, int m) {
  int product = 1;
  b = b % m;
  while ( e > 0) {
    if (e & 1) {
      product = modmult(product, b, m);
    }
    b = modmult(b, b, m);
    e >>= 1;
  }
  return product;
}
```





```
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```





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    }
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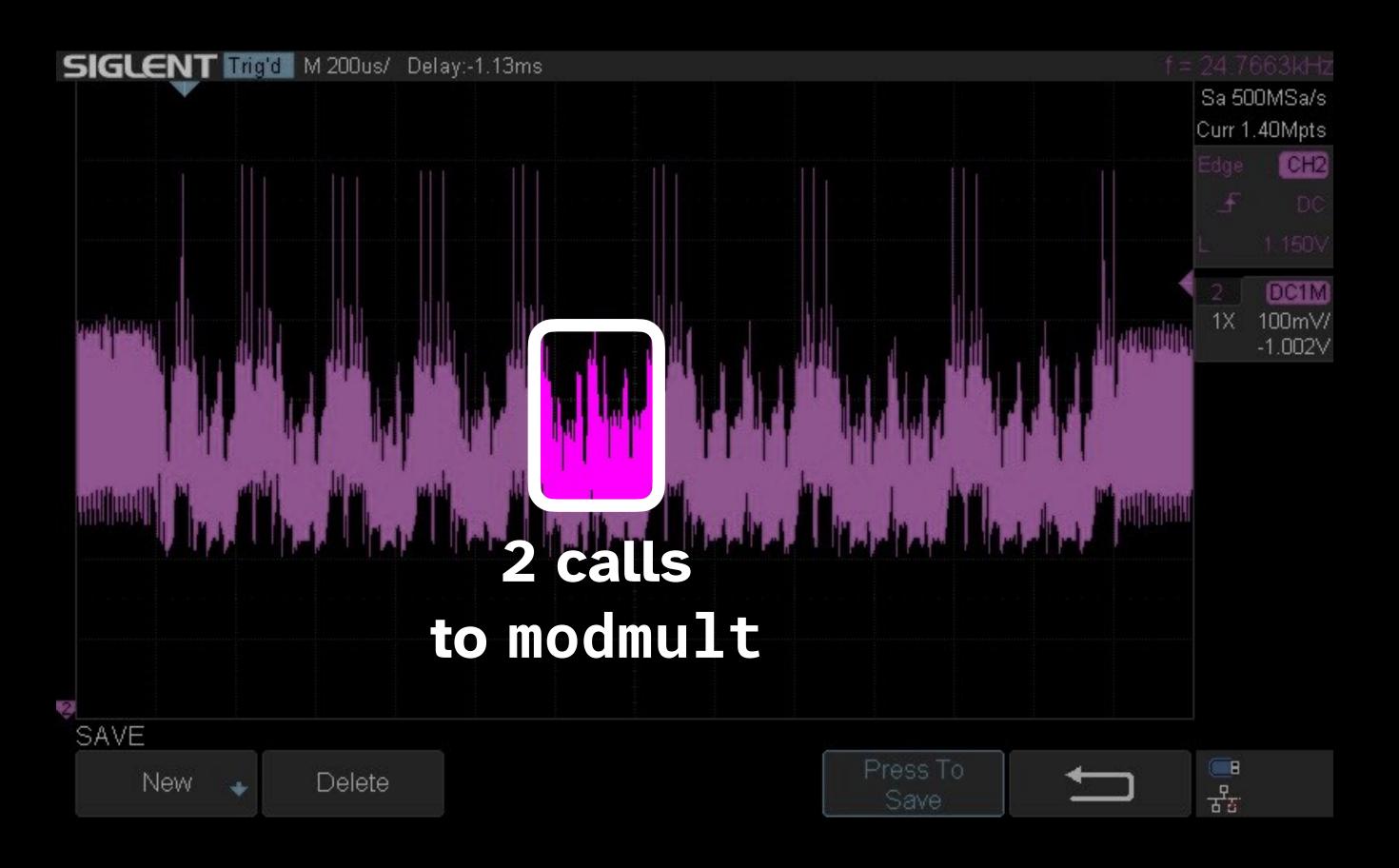
  e >>= 1;
  }
  return product;
}
```





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      product = modmult(product, b, m);
    }
    b = modmult(b, b, m);
    e >>= 1;
  }
  return product;
}
```

e = 0xf0

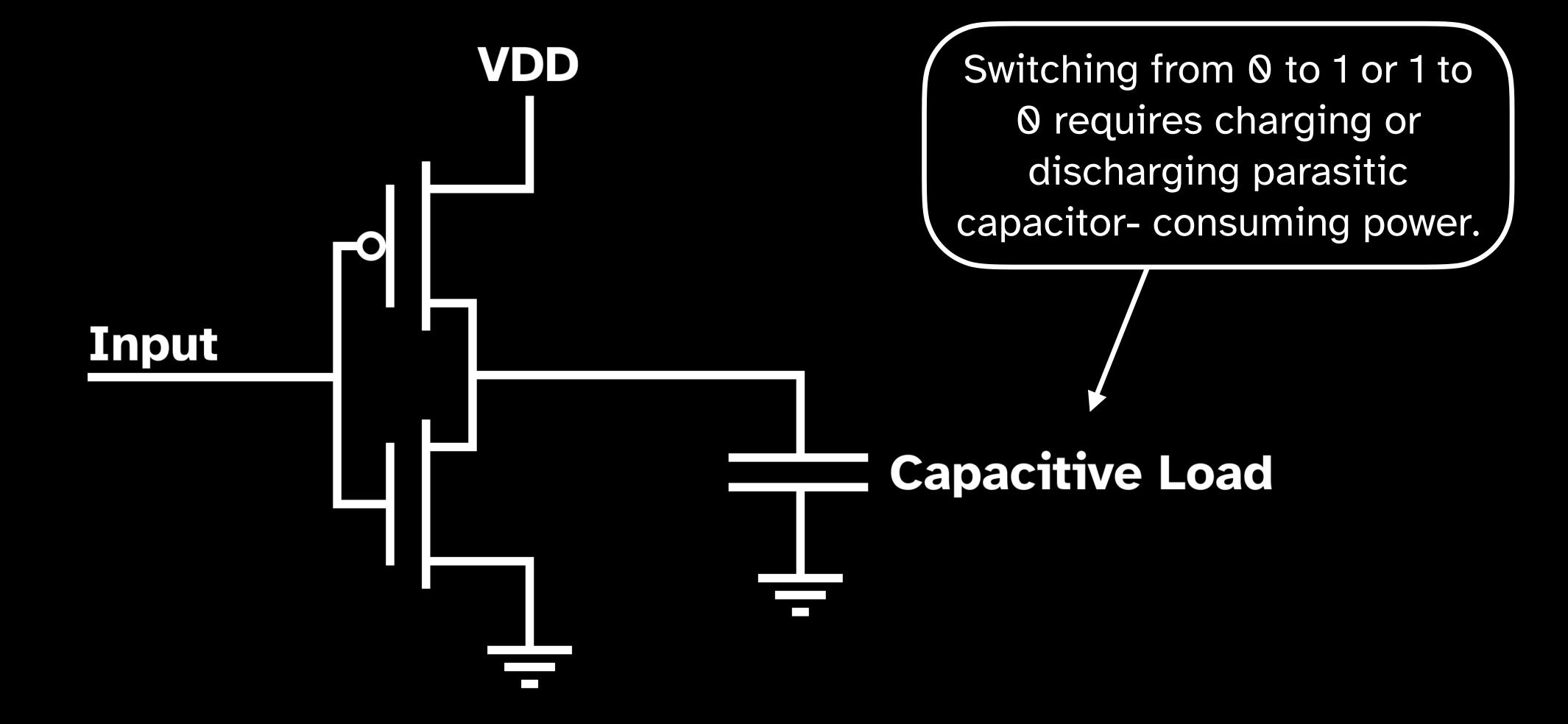


"What if we watch the chip's current draw?"

So, why does that work?

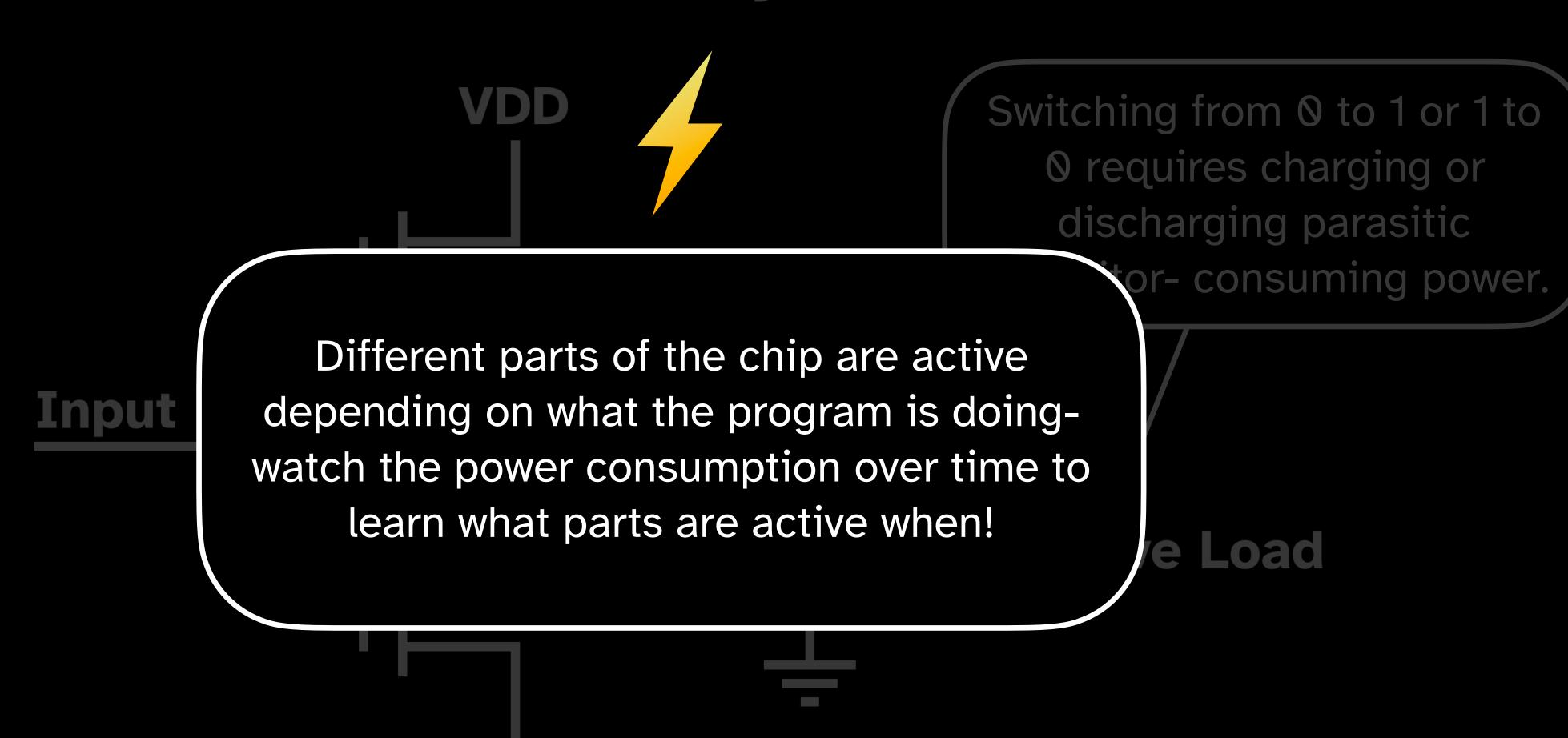


CMOS Inverter In Reality

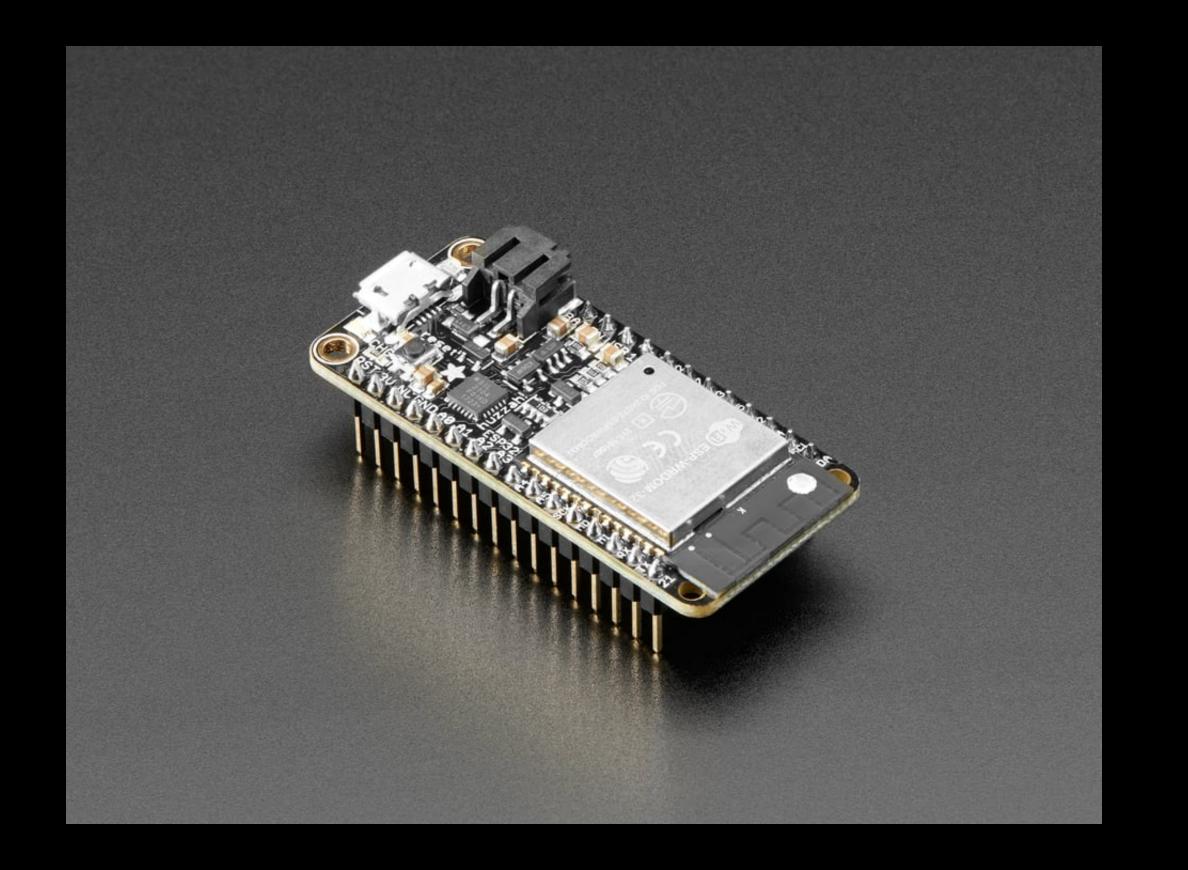




CMOS Inverter In Reality







Next: Your Turn...



Bring a USB Micro or USB-C cable if you have it.

Install the Arduino IDE as well-instructions will be posted on Piazza.

